Radiation hard electronics for HEP experiments: problems and solutions

Federico Faccio
CERN / EP-ESE-ME

Outline

Introduction to ASICs and CMOS technologies

Fundamentals of radiation effects

Radiation effects in CMOS technologies

A brief history of radiation-tolerant ASIC development for LHC

The first generation of LHC experiments: 0.25µm CMOS

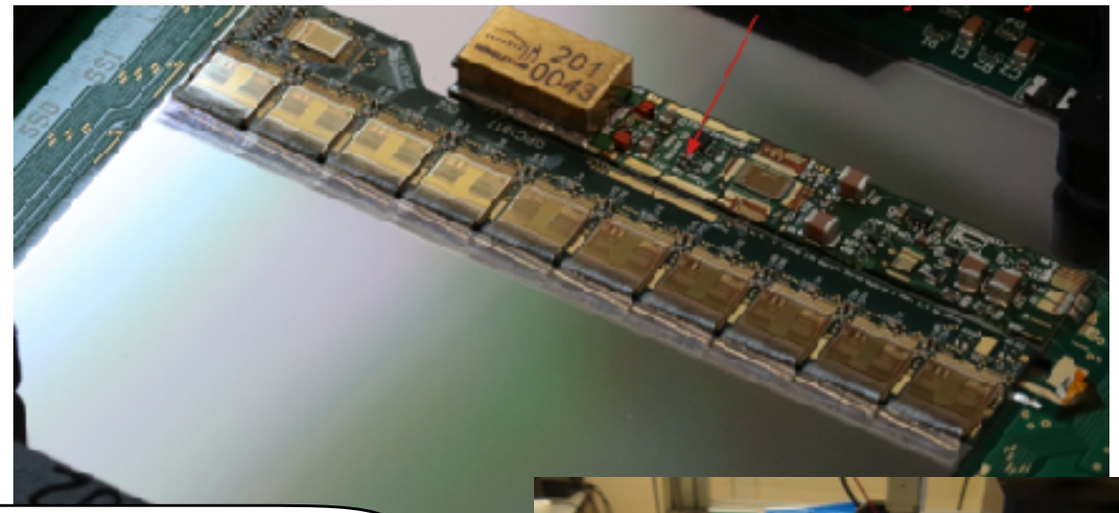
130nm CMOS for the upgrades

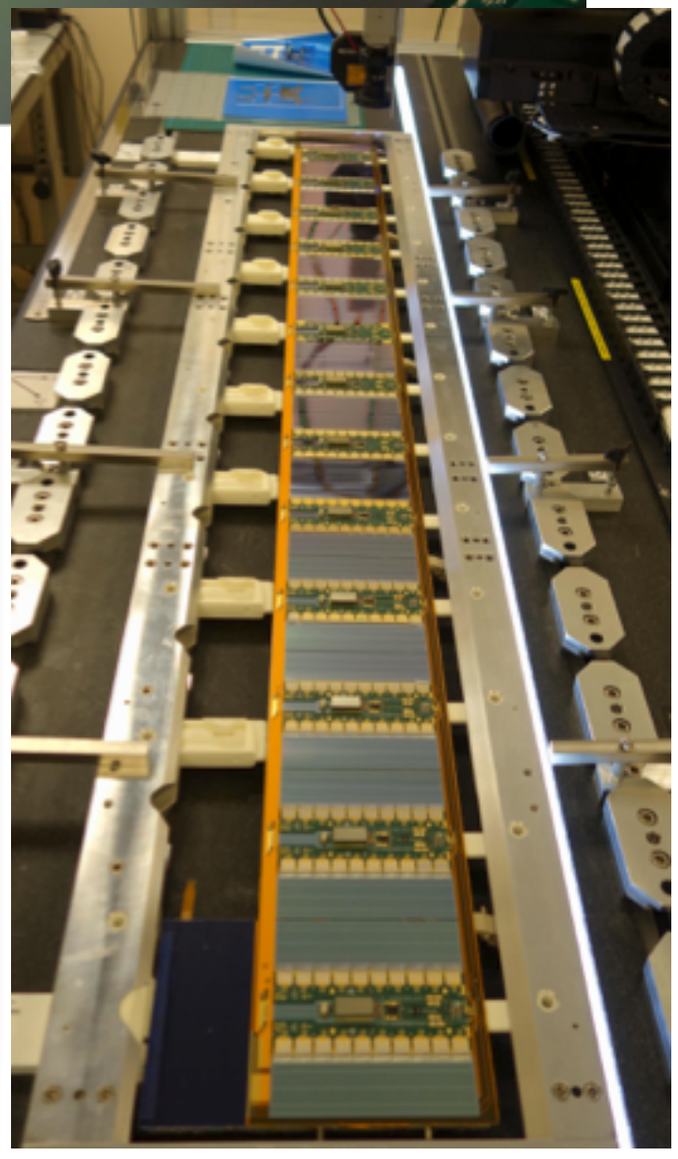
Higher radiation levels for HL-LHC: new effects

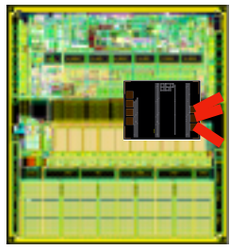
Case Studies

Application Specific Integrated Circuits (ASICs)

Integrated circuits (CHIPS) are used
in High Energy Physics experiments…







DC-DC converters

bPOL12V

Short Strip ASIC x 8

Concentrator IC (CIC)
Data aggregation

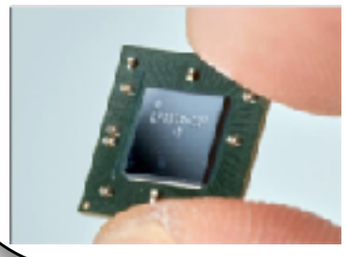
SSA

Strip Layer
~ 2k strips

Macro Pixel ASIC x 16

Pixelated Layer
~ 32k pixel

LP-GBT and VTRx+
Data transmission through the optical link

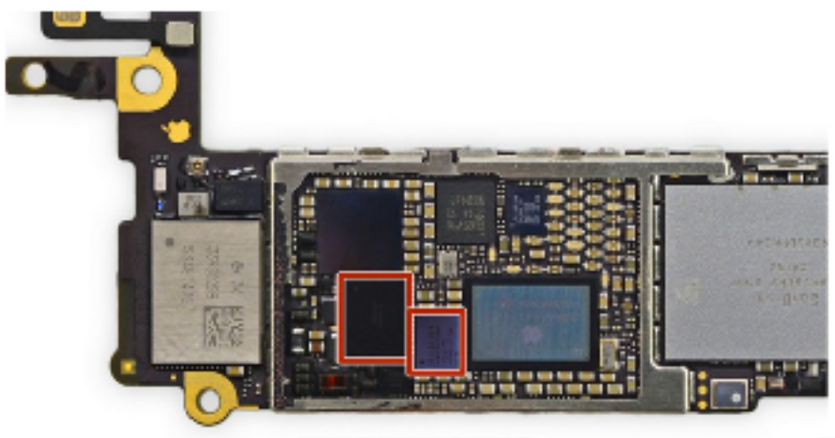


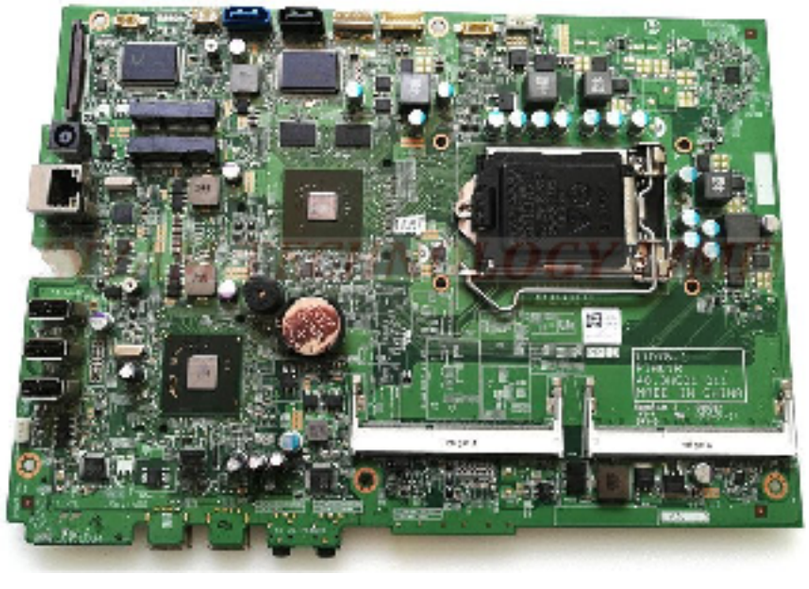
lpGBT

MPA

Integrated circuits (CHIPS) are used
in High Energy Physics experiments…

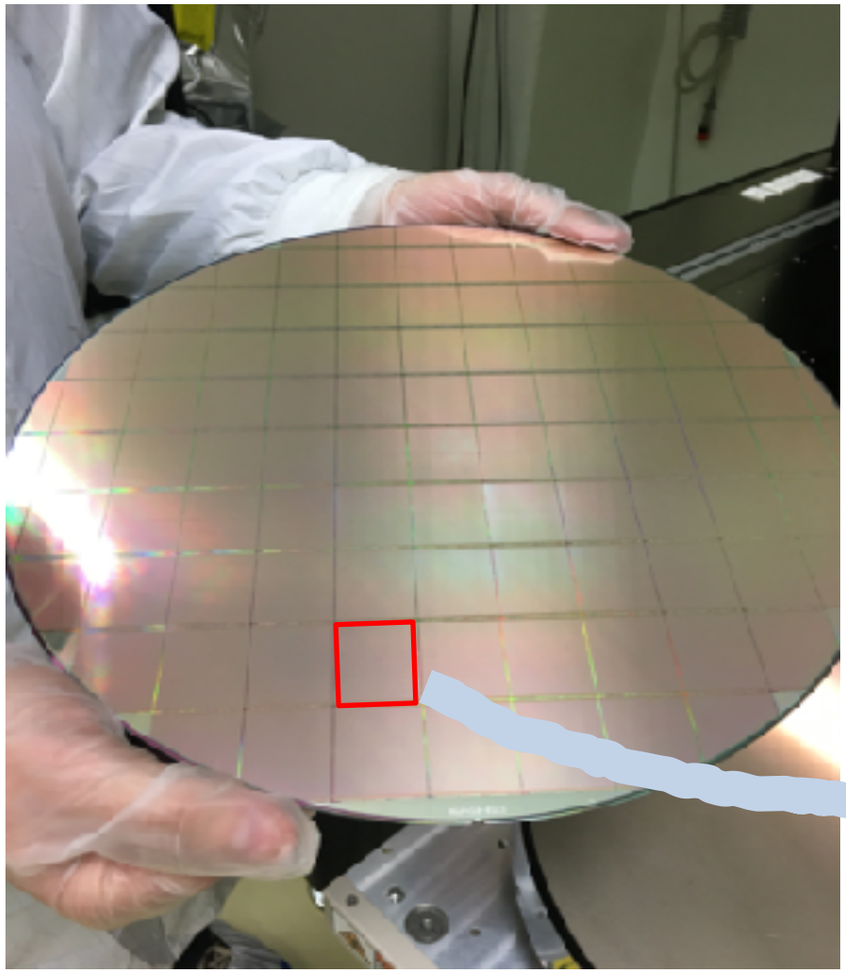
… but also in phones, PCs, domestic appliances, cars. Actually, everywhere!



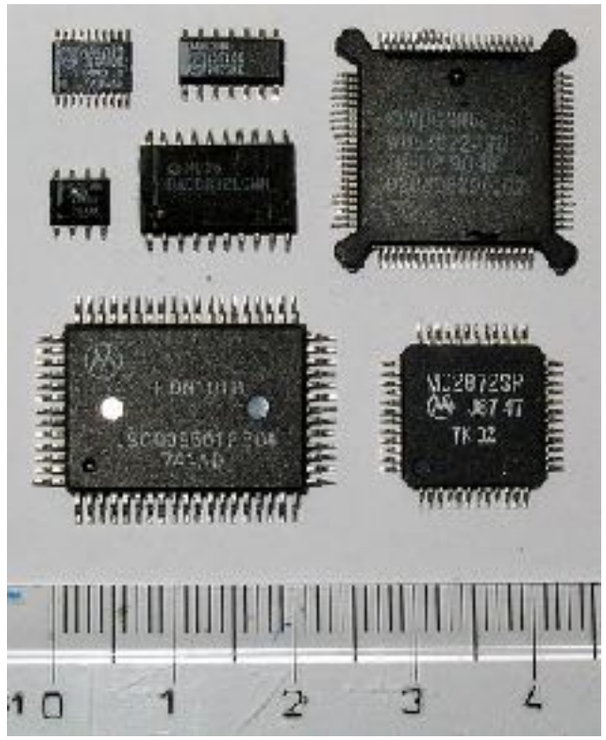


Inside the package

Integrated circuits (CHIPS) are manufactured on a silicon wafer, each containing a multitude of identical chips

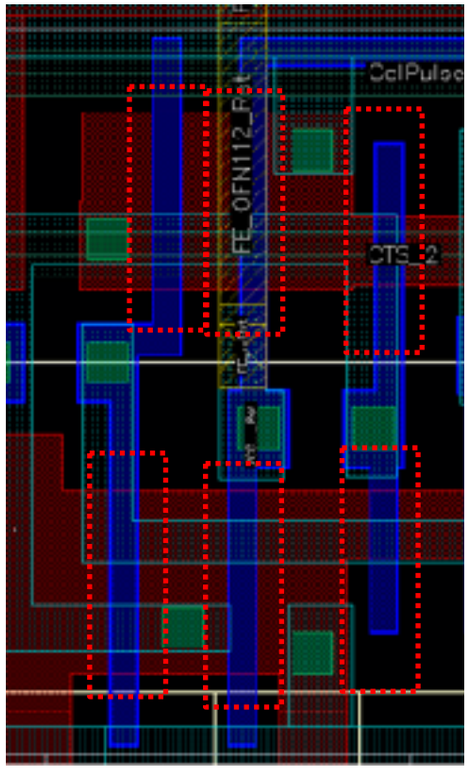


After wafer dicing, individual chips are most often assembled in a plastic package

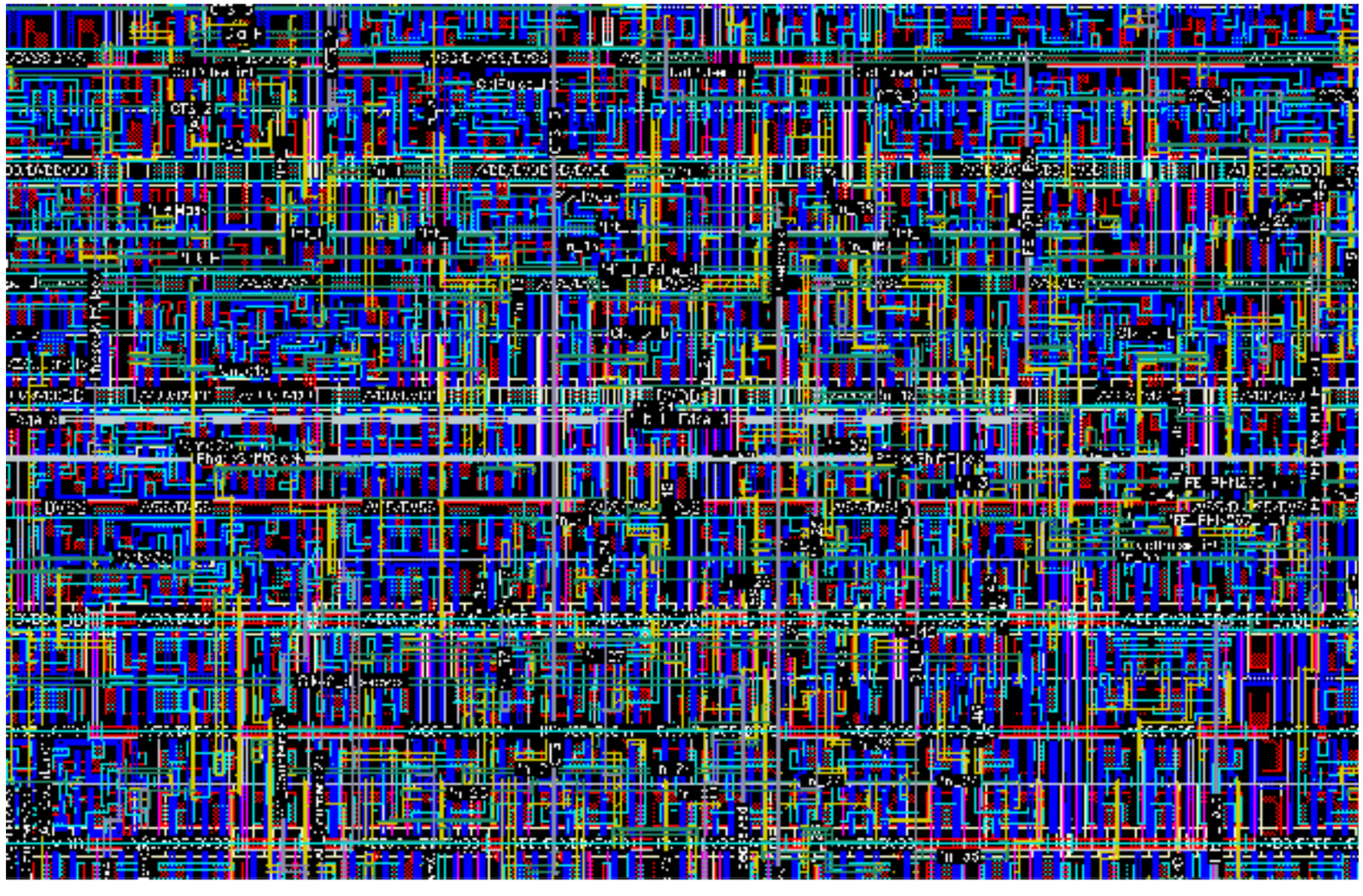


Transistors to make a CHIP

A CHIP is made up of transistors connected to form a circuit

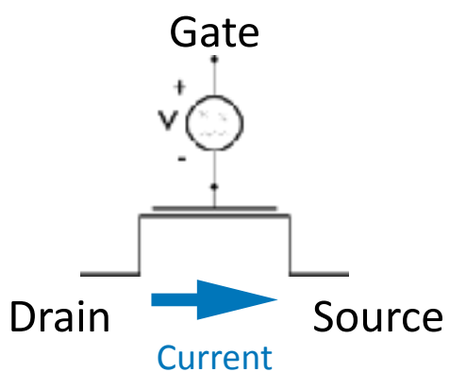


Drawing to manufacture
6 transistors
(in the red squares)

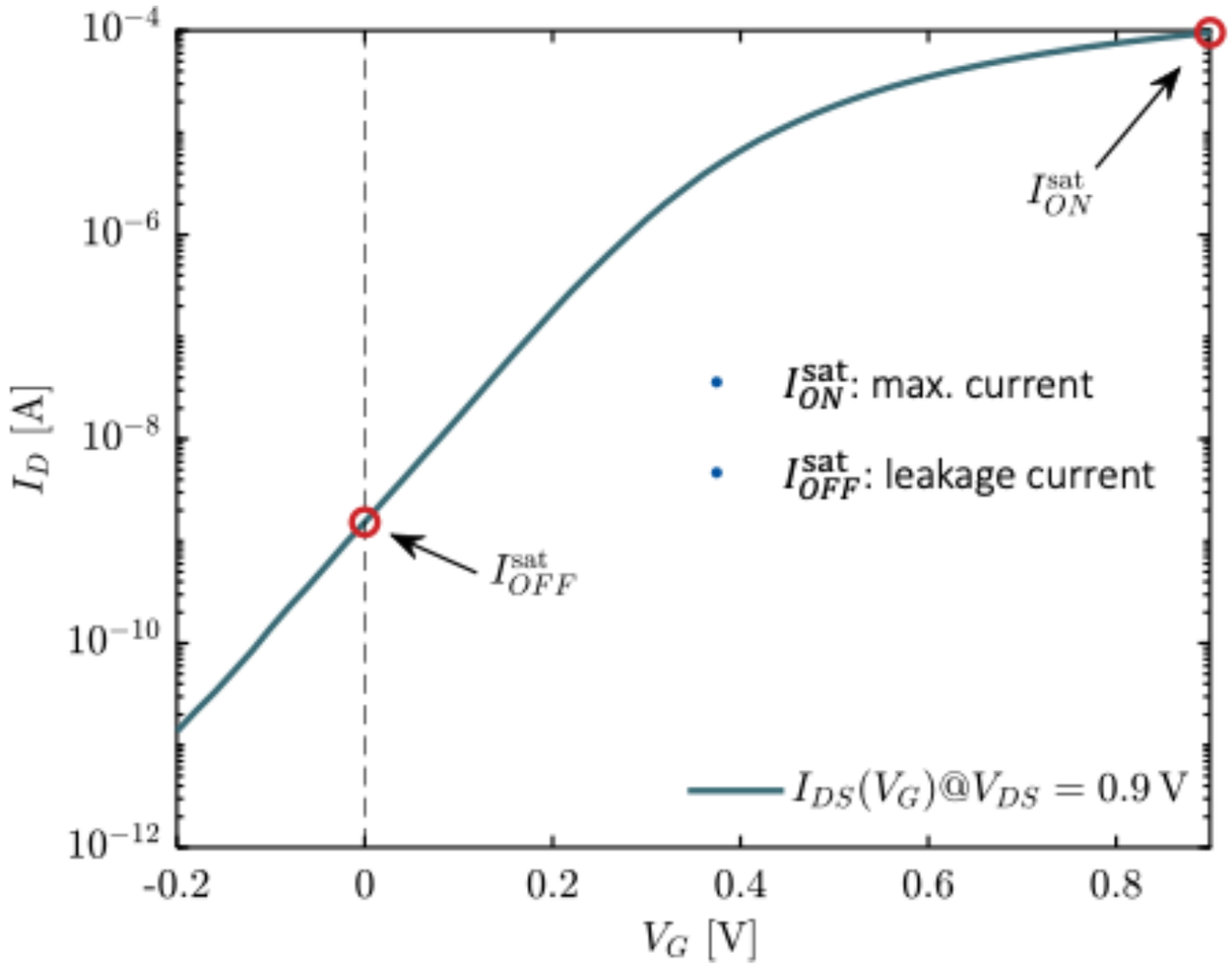


Thousands of transistors interconnected by metal lines

Transistors' drain-source current is controlled by the voltage applied to the gate and is proportional to the physical size (W/L, where W is the width and L the length)

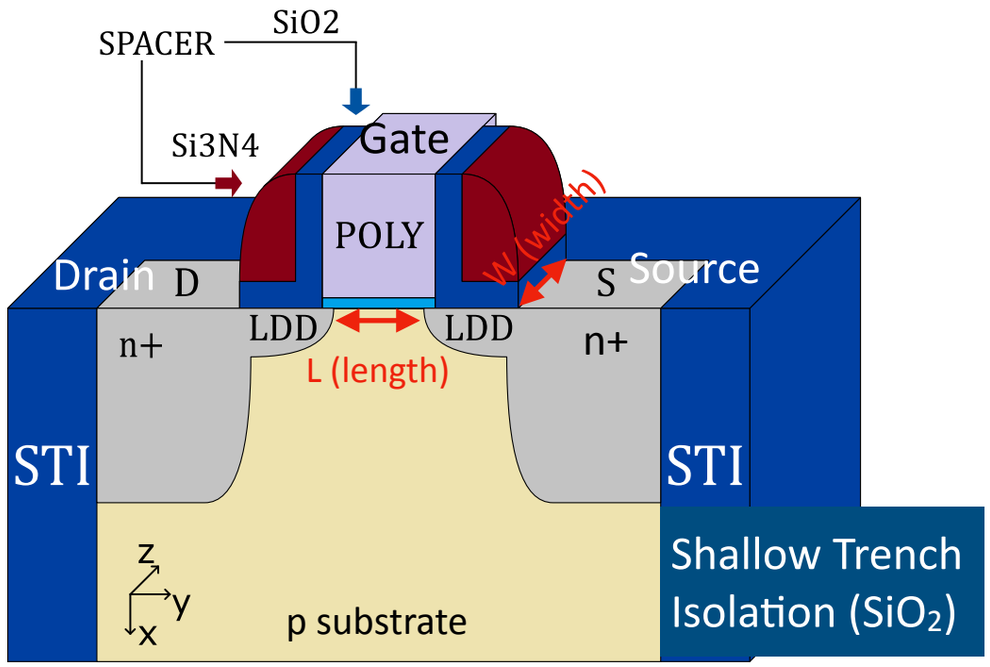


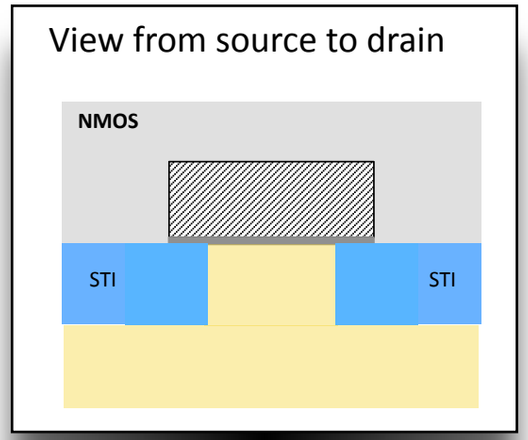
V_{Gate}	⇒	Control voltage
$I_{Drain-to-Source}$	⇒	Current

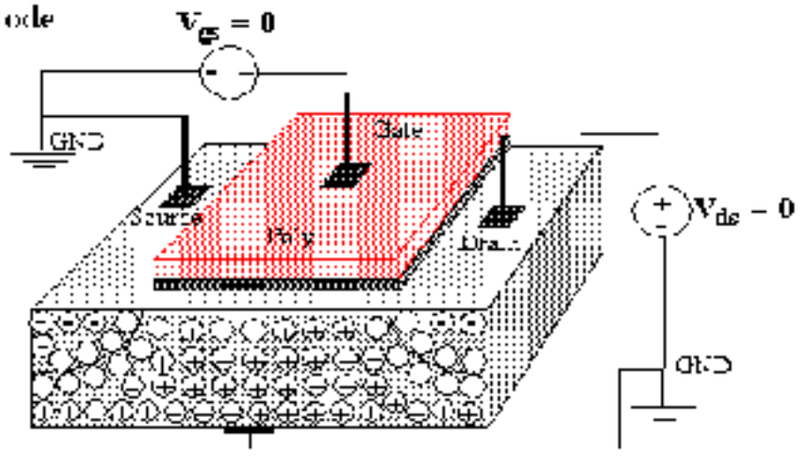


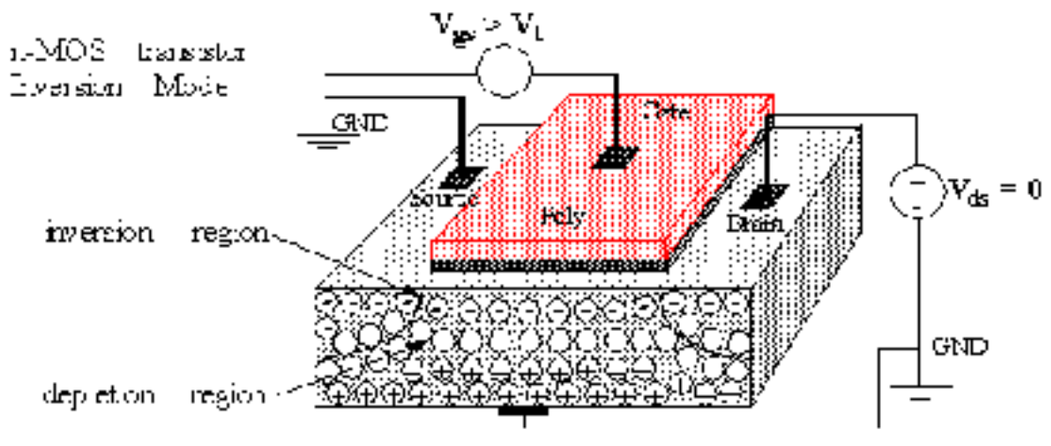
Transistors' drain-source current is controlled by the voltage applied to the gate and is proportional to the physical size (W/L, where W is the width and L the length)

N-channel transistor (NMOS)









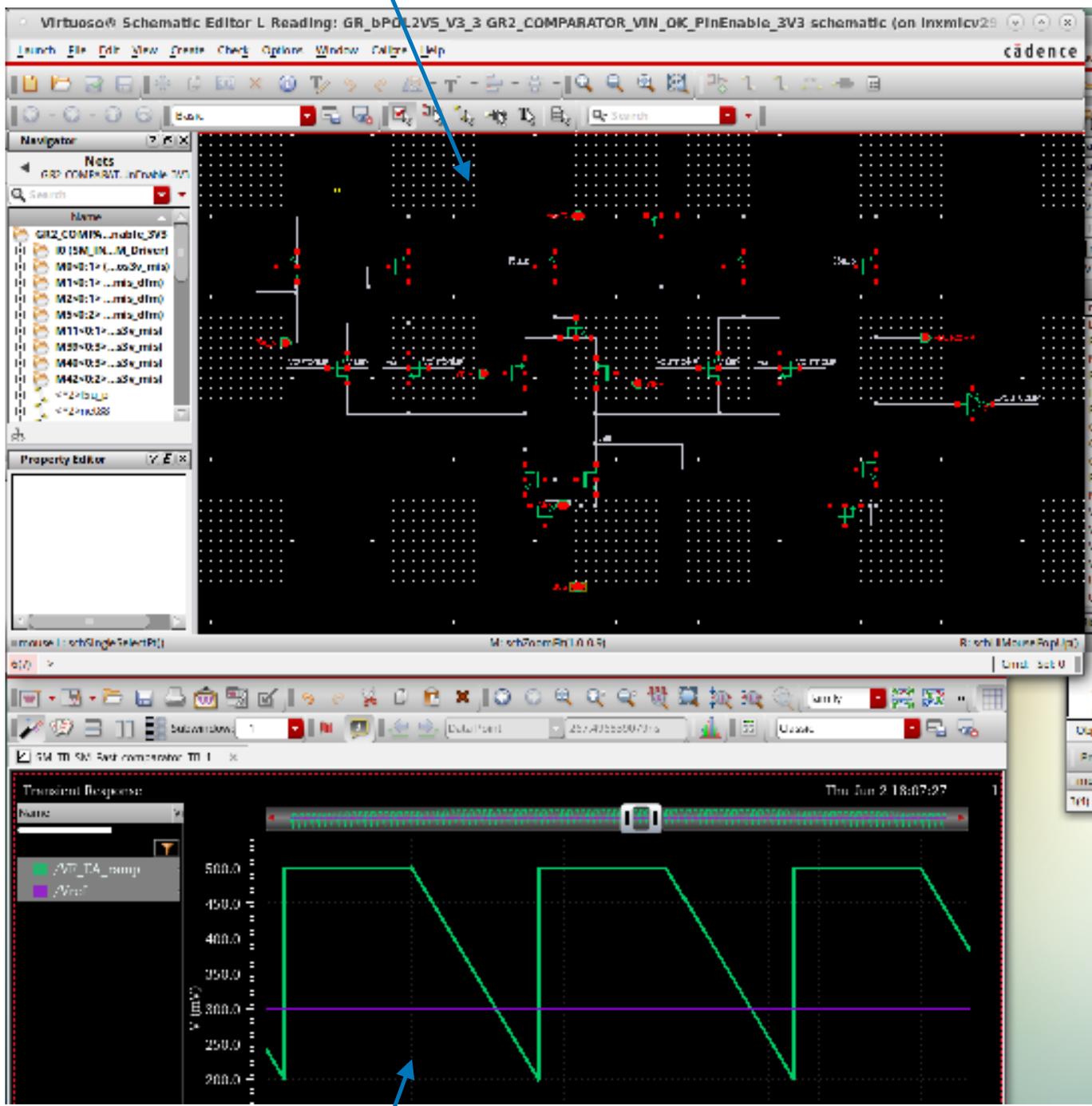
P-channel transistors (PMOS) are the same
but they have reverse polarity (n and p doped regions are inverted)

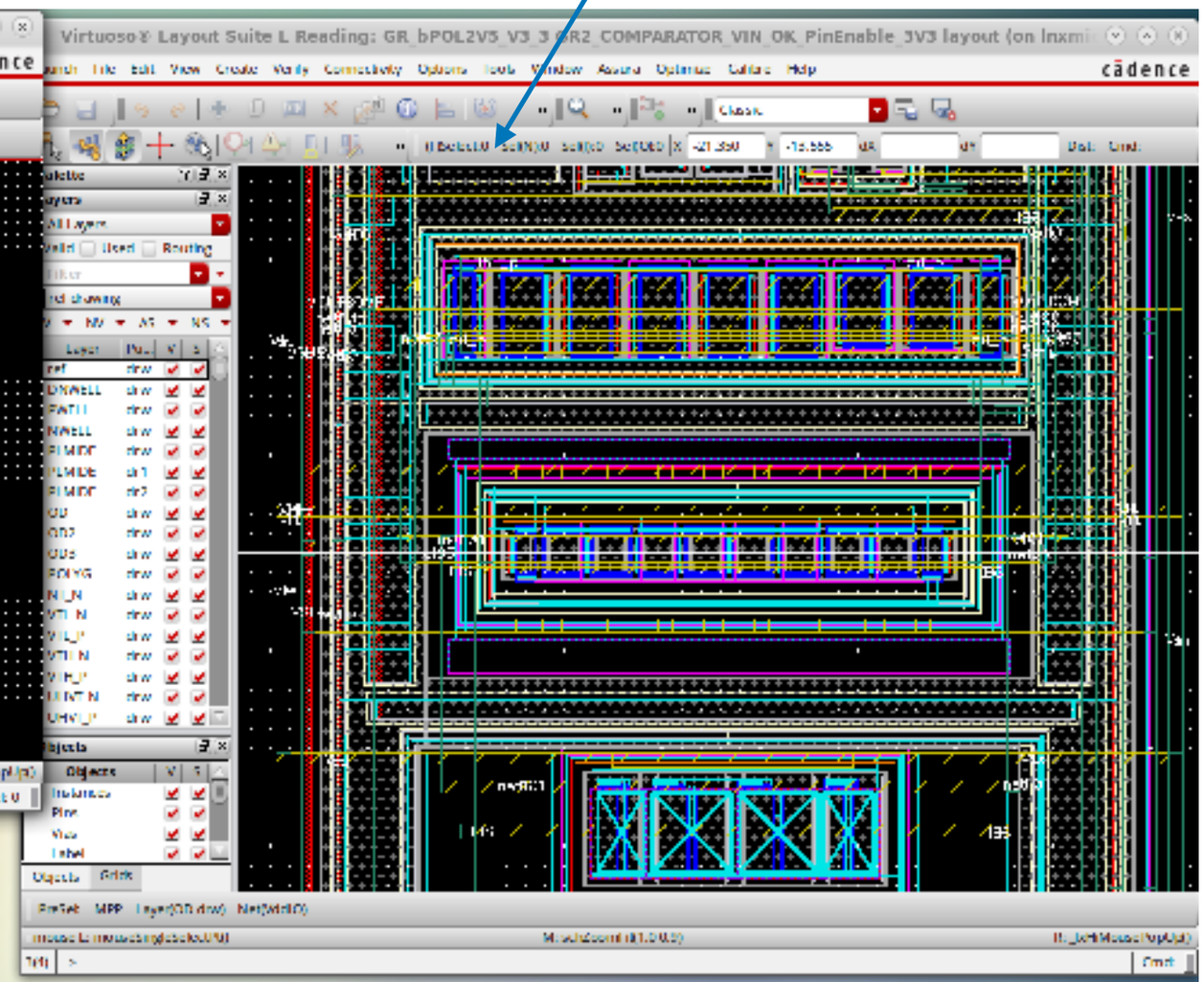
CMOS technologies use both NMOS and PMOS transistors

Connecting transistors to form a circuit: analog design

Schematic: plan of the connection scheme

Layout: plan for the manufacturing (masks)



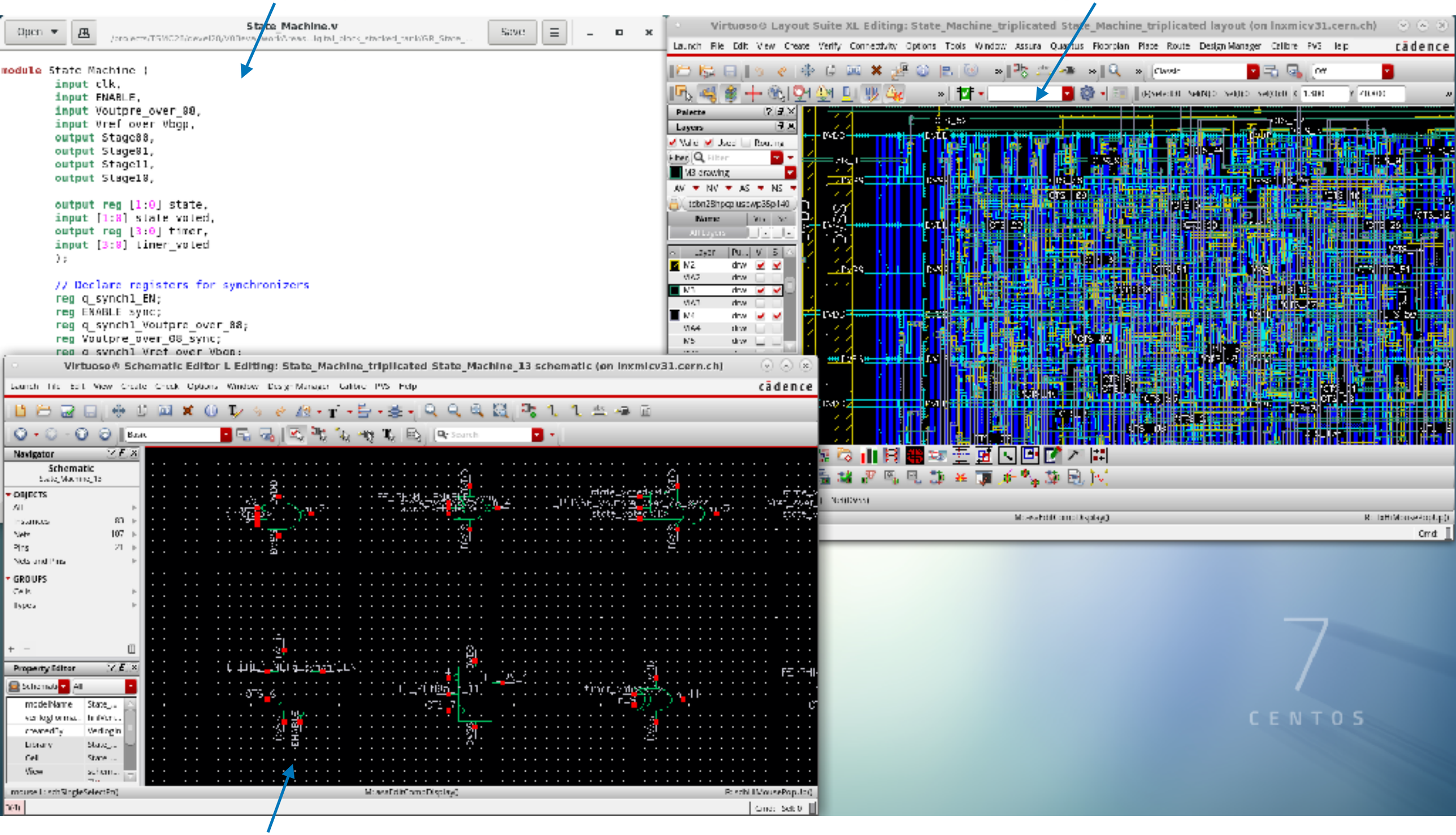


Simulation of the schematic: waveforms

Connecting transistors to form a circuit: high-level digital design

Code: functional description of the circuit

Layout: plan for the manufacturing (masks)
Automatically generated

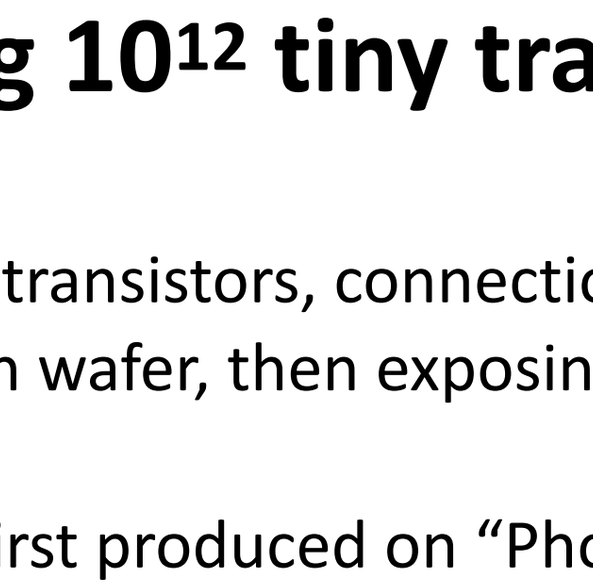


Blocks used by the automatic generator
(pre-existing in a library with physical description and electrical parameters)

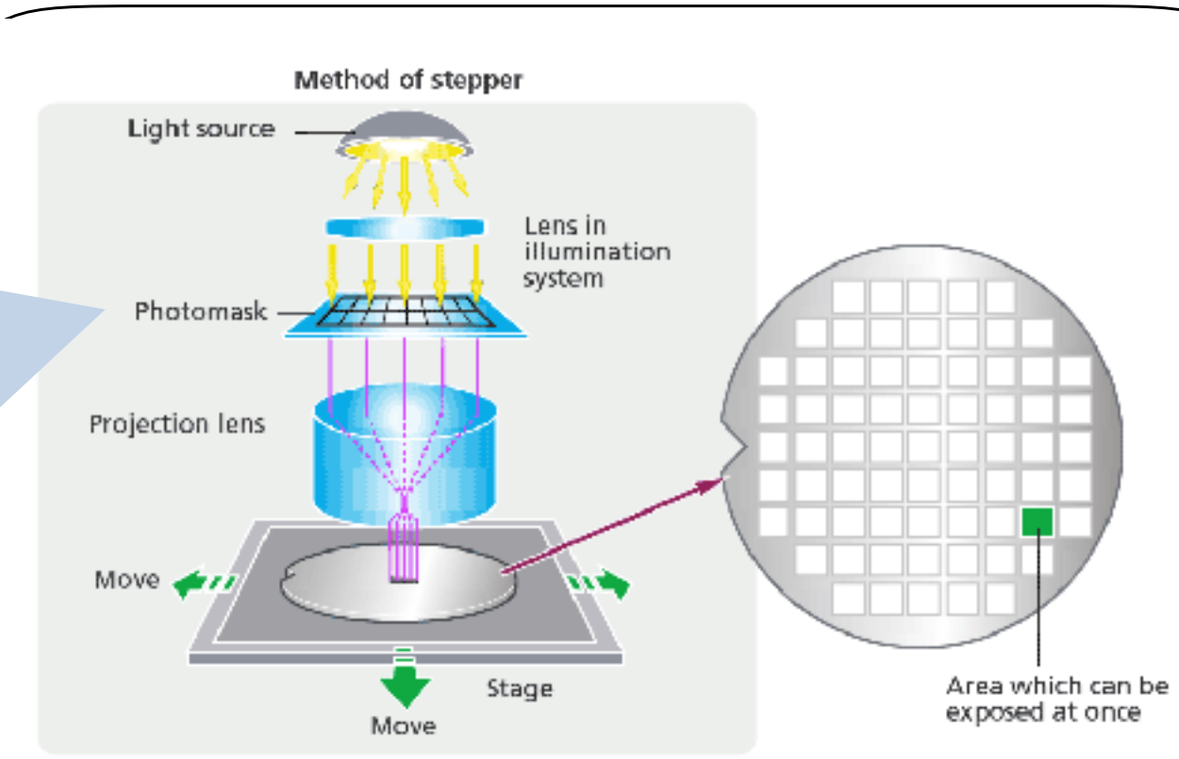
Printing 10^{12} tiny transistors in a CHIP

All features (transistors, connection lines, …) are manufactured by “printing” features on the silicon wafer, then exposing the printed zones to specific processing steps.

Images are first produced on “PhotoMasks”, then printed – on a much smaller size – on the wafer using very complex lithographic steps



”PhotoMask” used in IC manufacturing



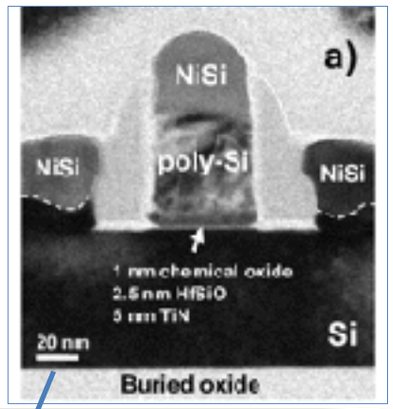
Silicon Wafer Manufacturing

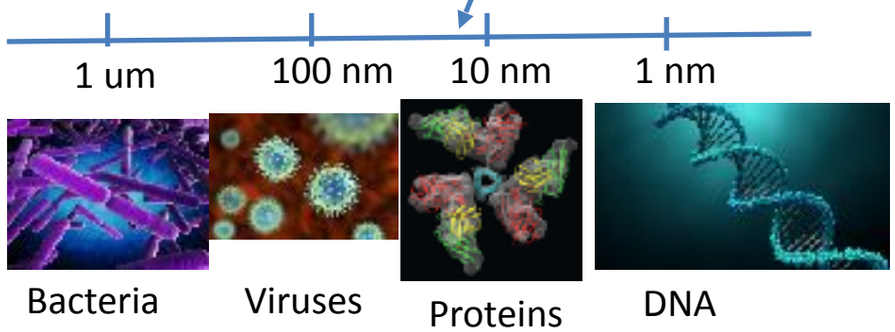
A giant to make a tiny dot

Throughput ~ 2500 wafers/day,
each with 7-70 Trillion MOS transistors

Aerial view of a manufacturing site (“FAB”)
where silicon wafers are produced

Transmission-Electron Microscope view of a single MOS transistor

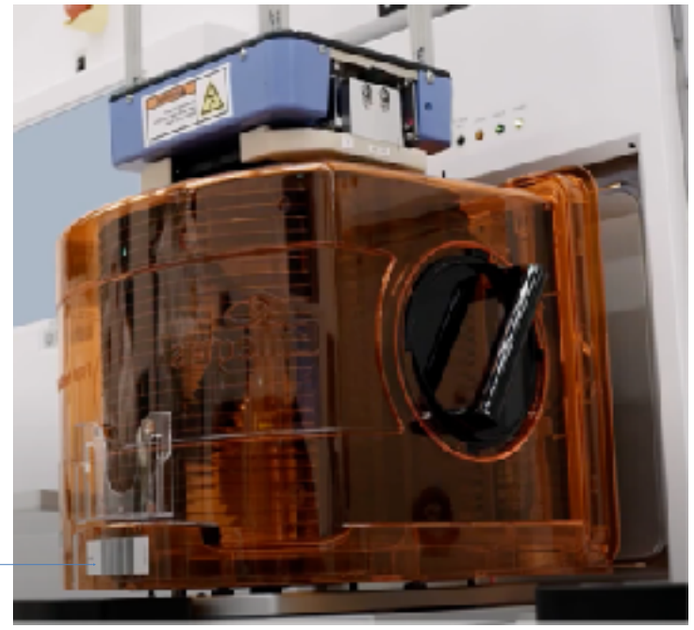




Silicon Wafer Manufacturing

Look inside a giant “FAB”

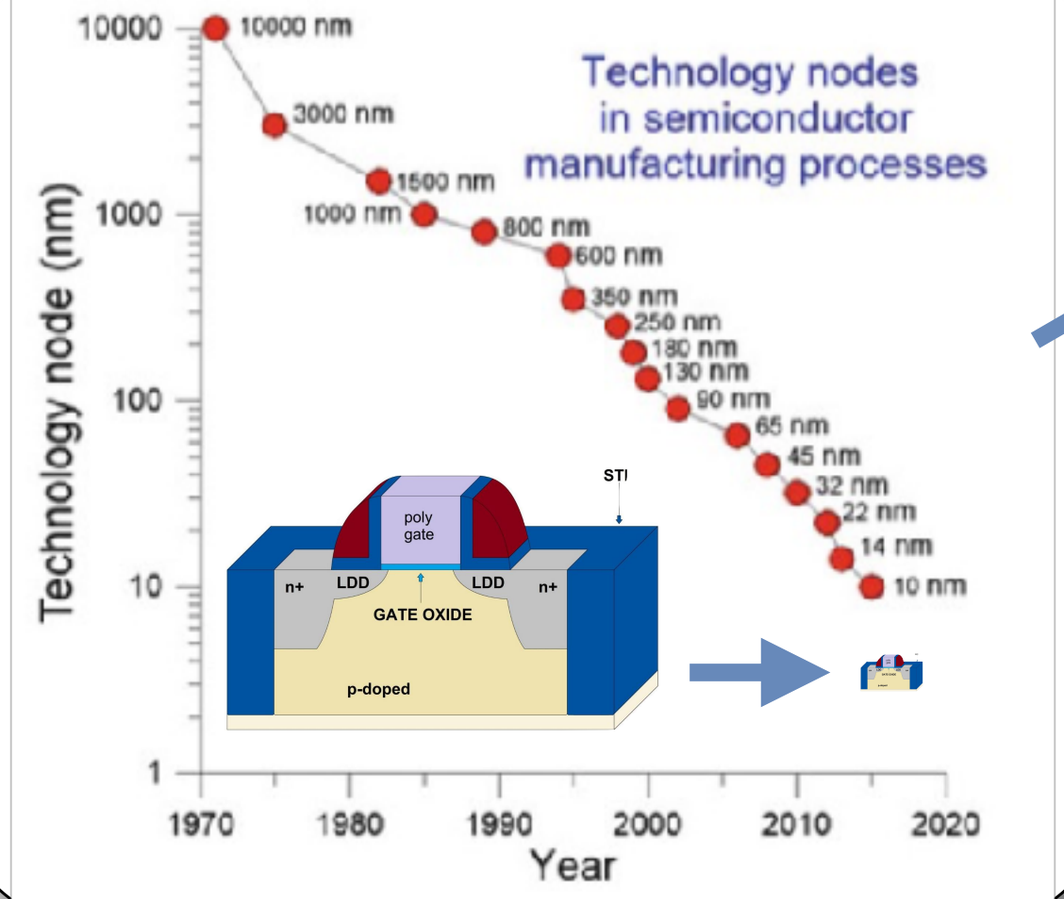
Wafers travel
through processing
equipment
in sealed vessels



Very few human operators are needed

The semiconductor industry has strived to scale the size of the CMOS transistors to smaller dimensions

Each generation is characterised by the minimum printable shape (called technology “Node”)

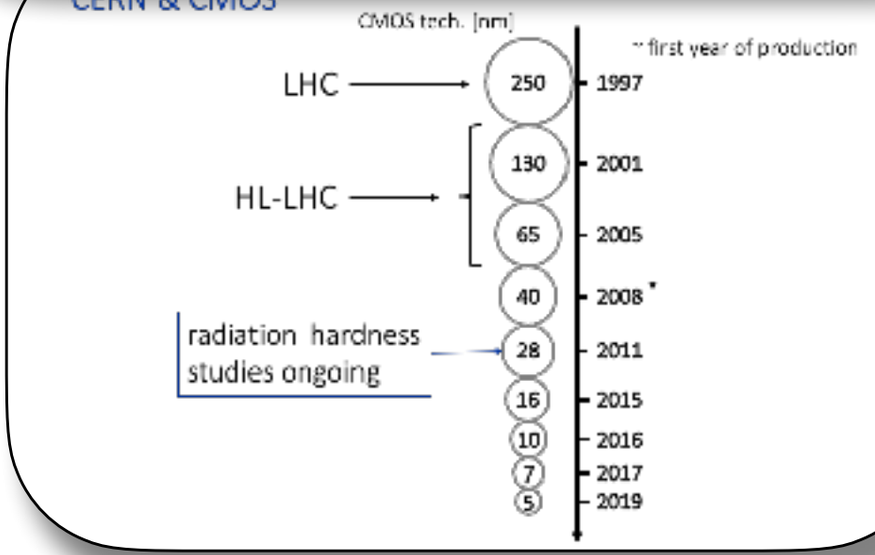


smaller transistor = higher performance; lower power; higher integration

Flash memory

Chip name	Capacity (bits)	Flash type	FGMOS transistor count	Date of introduction
7	256 Kb	NOR	262,144	1985
	1 Mb	NOR	1,048,576	1989
	4 Mb	NAND	4,194,304	1989
	16 Mb	NOR	16,777,216	1991
DD28F032SA	32 Mb	NOR	33,554,432	1993
	64 Mb	NOR	67,108,864	1994
		NAND	67,108,864	1996
	128 Mb	NAND	134,217,728	1996
	256 Mb	NAND	268,435,456	1999
	512 Mb	NAND	536,870,912	2000
?	1 Gb	2-bit NAND	536,870,912	2001
	2 Gb	NAND	2,147,483,648	2002
	8 Gb	NAND	8,589,934,592	2004
	16 Gb	NAND	17,179,869,184	2005
	32 Gb	NAND	34,359,738,368	2006
THGAM	128 Gb	Stacked NAND	128,000,000,000	April 2007
THGBM	256 Gb	Stacked NAND	256,000,000,000	2008
THGBM2	1 Tb	Stacked 4-bit NAND	256,000,000,000	2010
KLMCG8GE4A	512 Gb	Stacked 2-bit NAND	256,000,000,000	2011
KLUFG8R1EM	4 Tb	Stacked 3-bit V-NAND	1,365,333,333,504	2017
eUFS (1 TB)	8 Tb	Stacked 4-bit V-NAND	2,048,000,000,000	2019

CERN & CMOS



Outline

Introduction to ASICs and CMOS technologies

Fundamentals of radiation effects

Radiation effects in CMOS technologies

A brief history of radiation-tolerant ASIC development for LHC

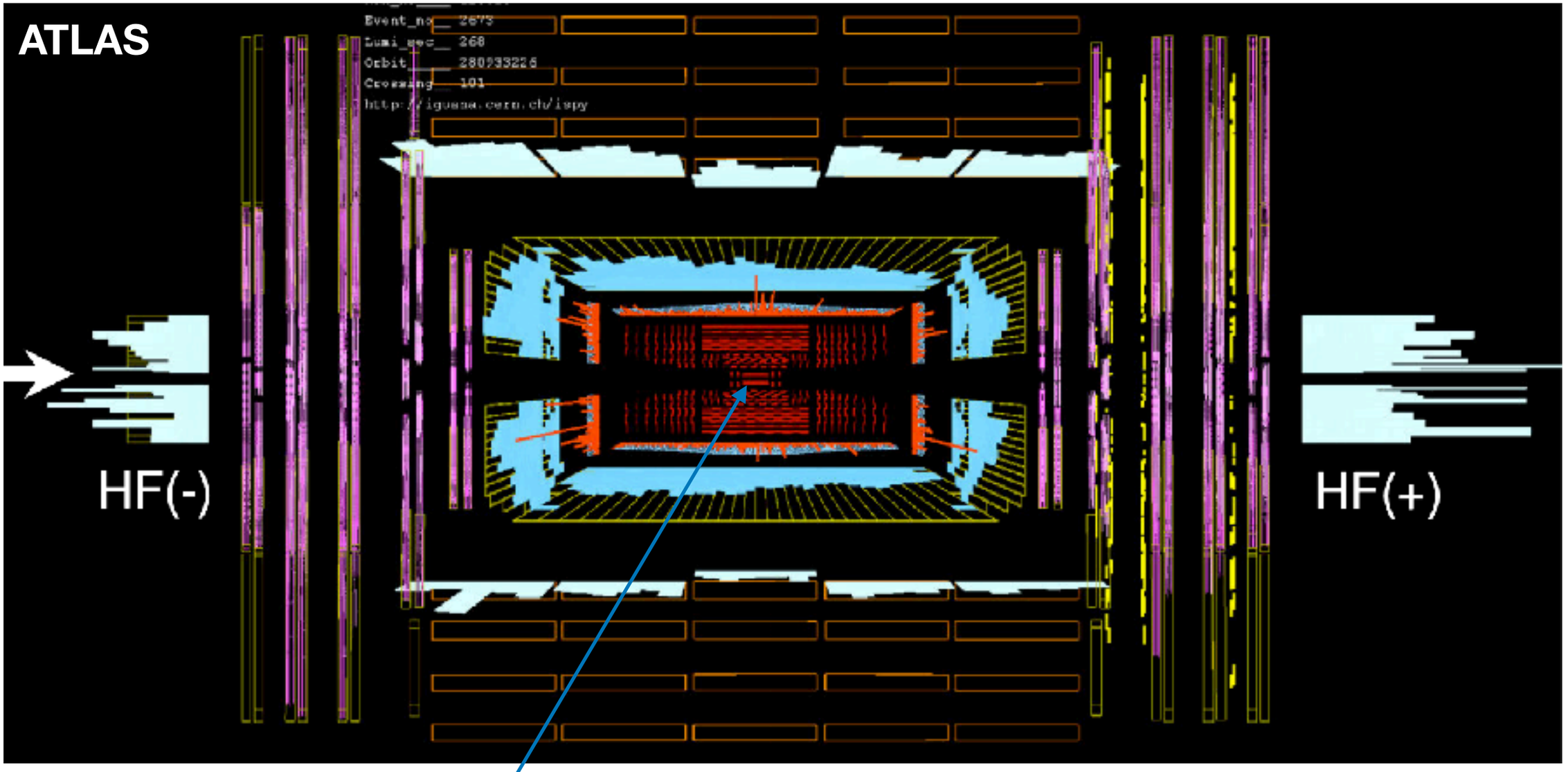
The first generation of LHC experiments: 0.25µm CMOS

130nm CMOS for the upgrades

Higher radiation levels for HL-LHC: new effects

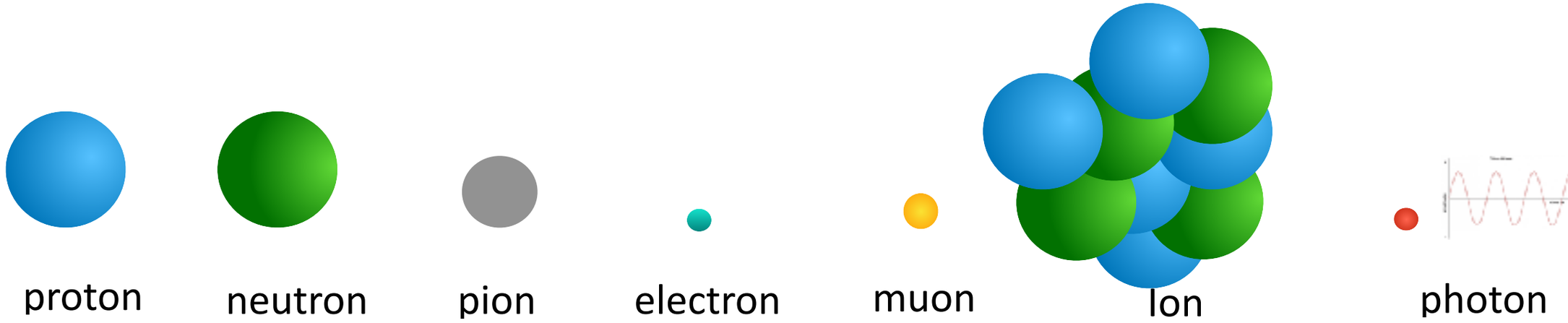
Case Studies

The electronics in the LHC experiments is immersed in a radiation field generated by the p-p collisions at their center.

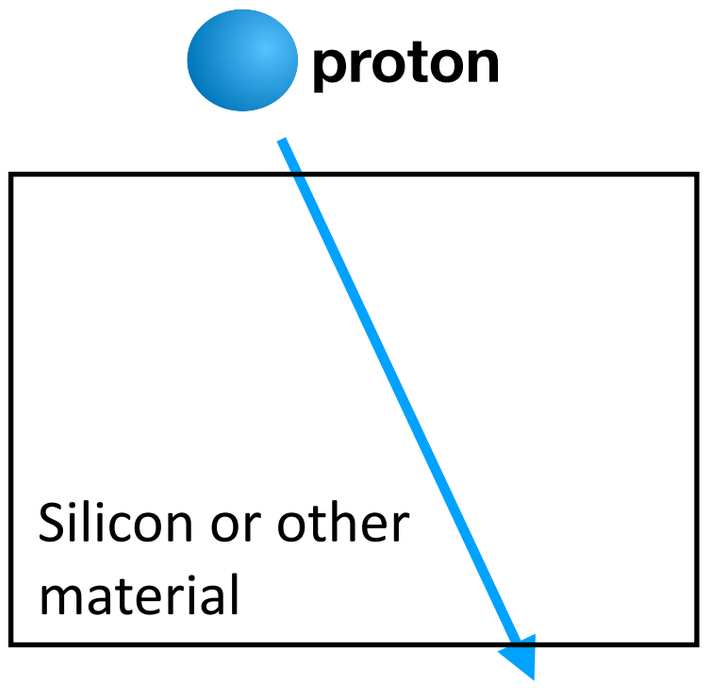


Collisions at the center: the radiation field is more intense in the inner detector layers and decreases with the distance.

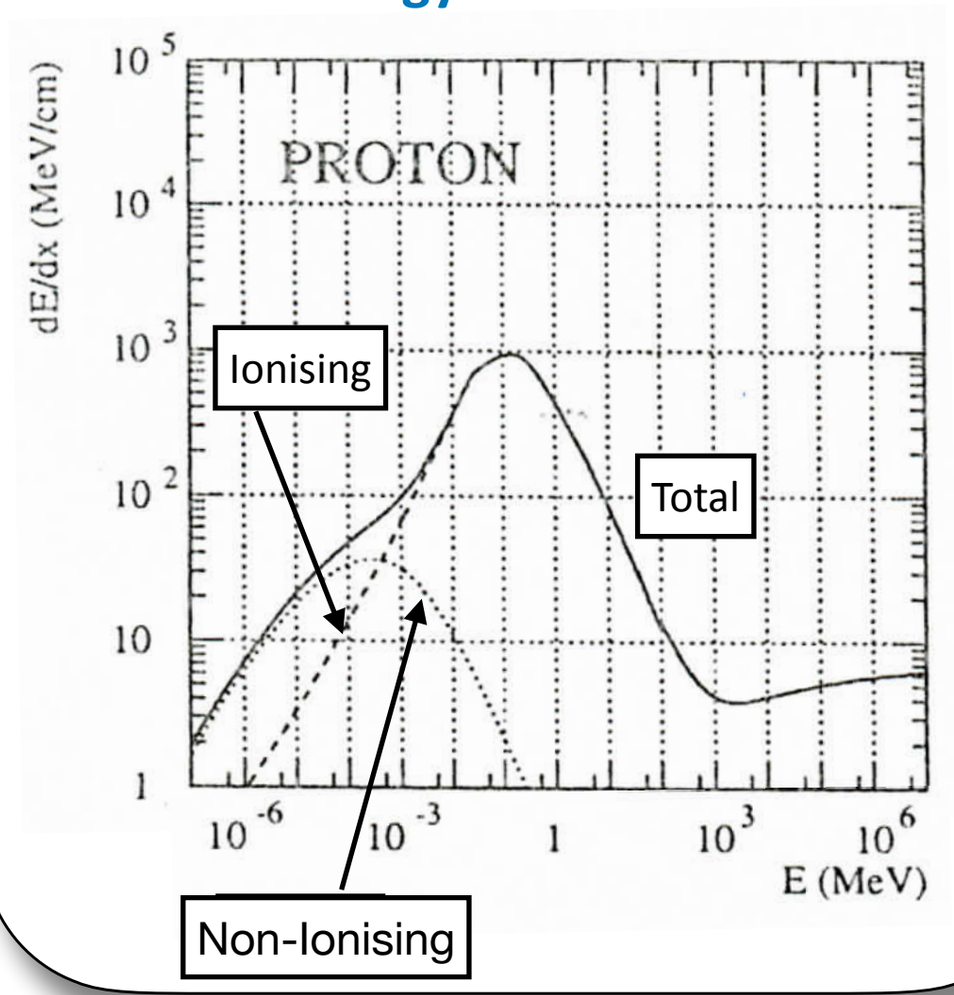
Main particles responsible for radiation effects in semiconductor materials



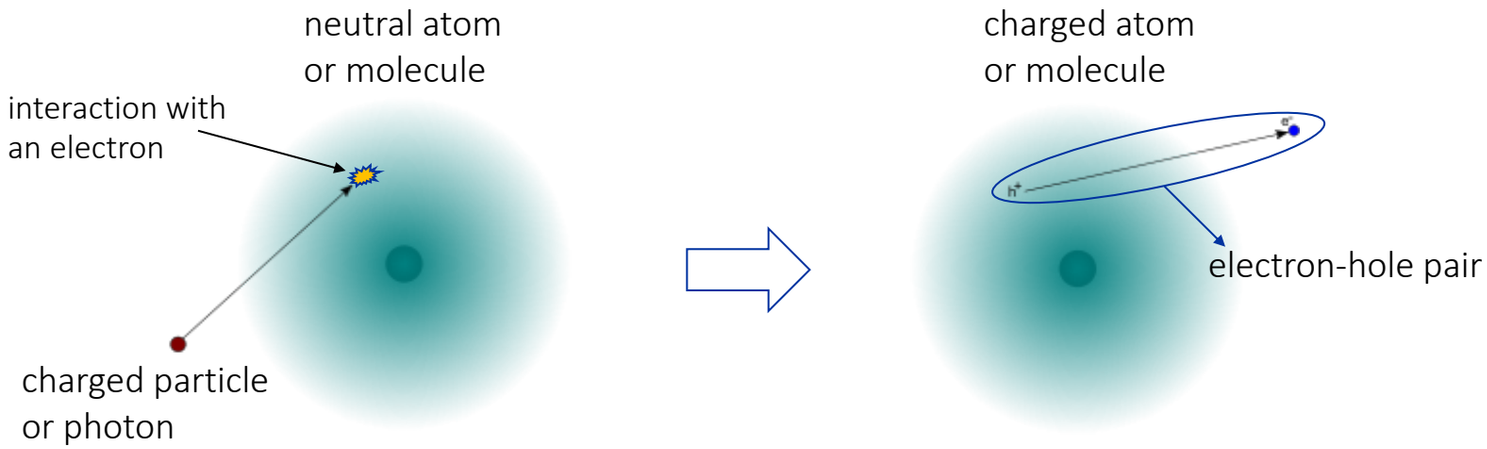
Energetic protons interact with atoms in the material they traverse.
They can loose energy per unit path length via ionising or non-ionising processes.



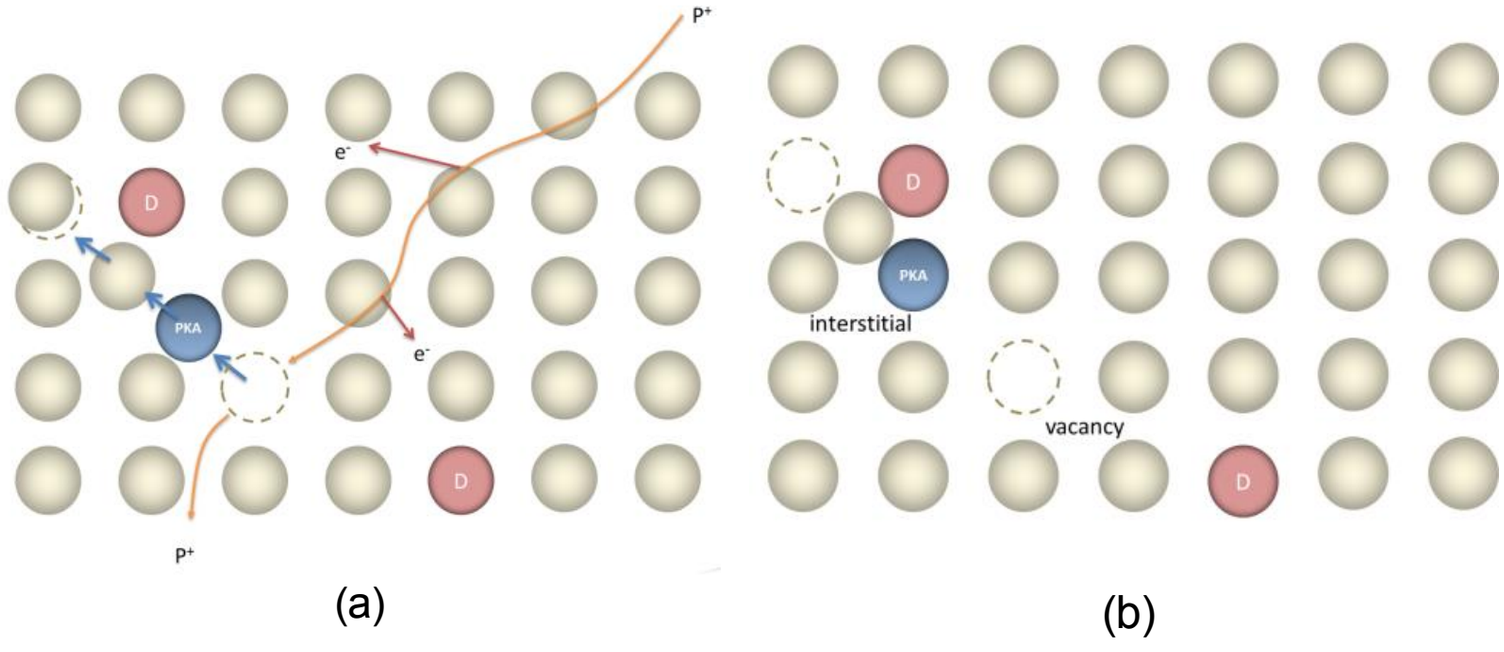
Energy loss in Silicon



Ionising Energy Loss:
electron-hole pair creation

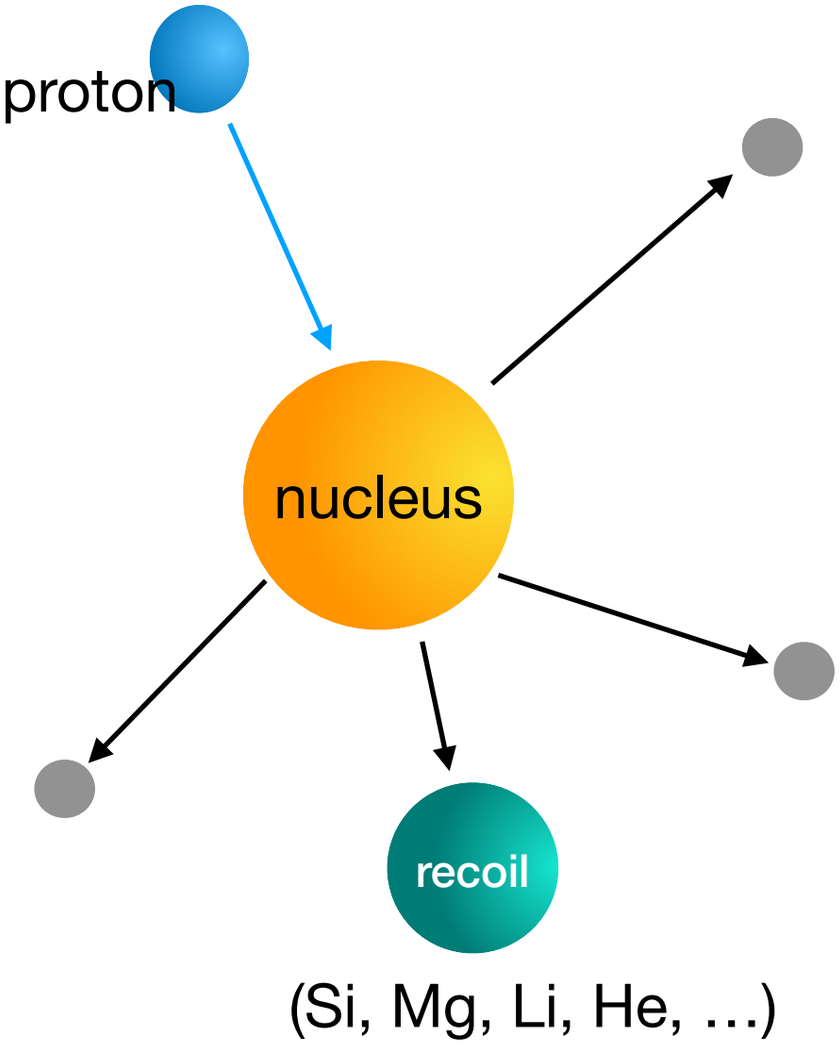


Non-Ionising Energy Loss (NIEL):
atoms are displaced from their regular position in the lattice, giving origin to interstitials and vacancies.
The disturbance in the crystal lattice periodicity has associated discrete energy levels in the forbidden energy band-gap. These influence generation-recombination processes in the material.

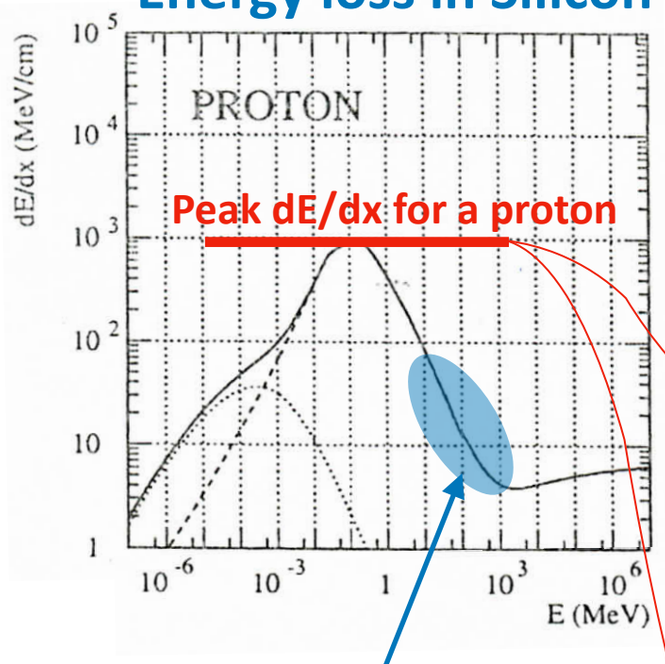


after C.Virmontois, “Displacement Damage in optoelectronic devices for space applications”, Short Course at the 2017 RADECs, Geneva

Neutrons, protons and pions can also interact with the nuclei of the material
(if their energy is sufficient to overcome the repulsive electrostatic barrier of the nuclei).
Typically this will produce a shower of secondary particles and one nuclear recoil (Si, Mg, Li, He, …) with much higher dE/dx and small range.

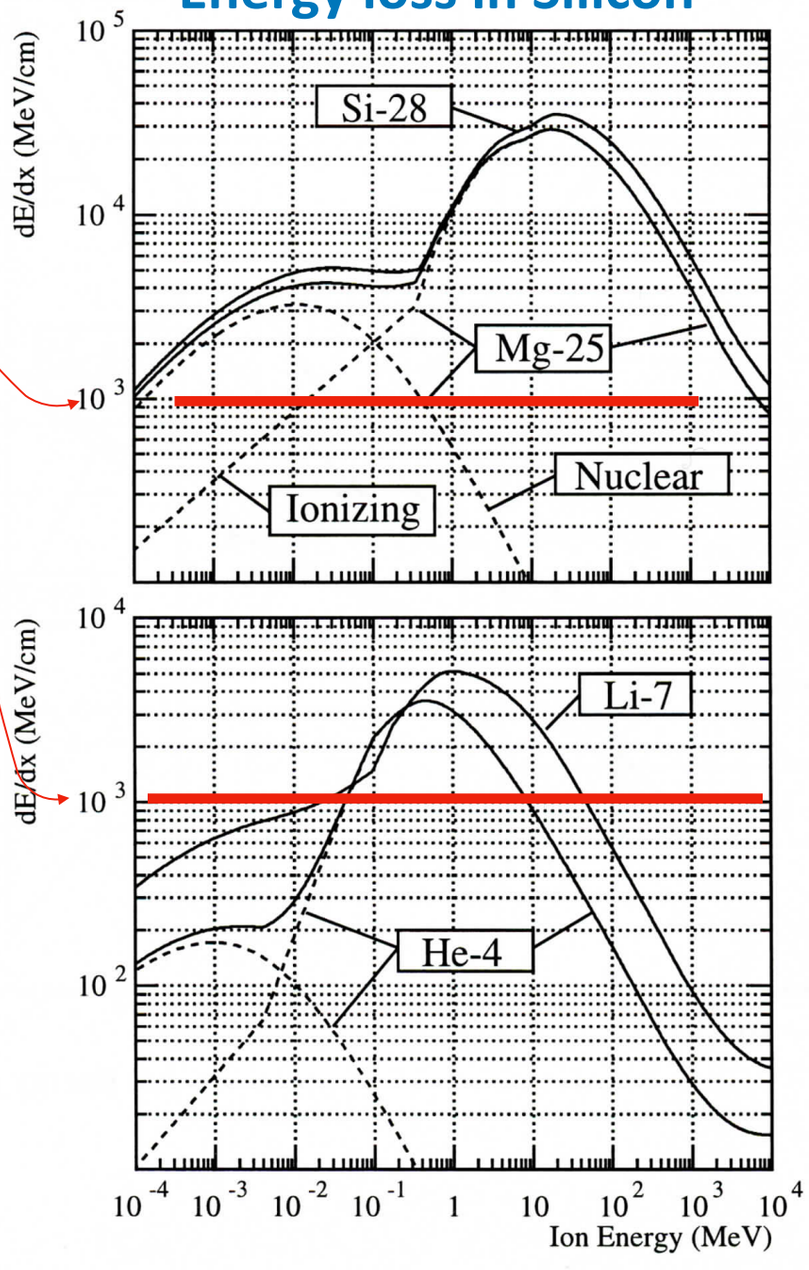


Energy loss in Silicon

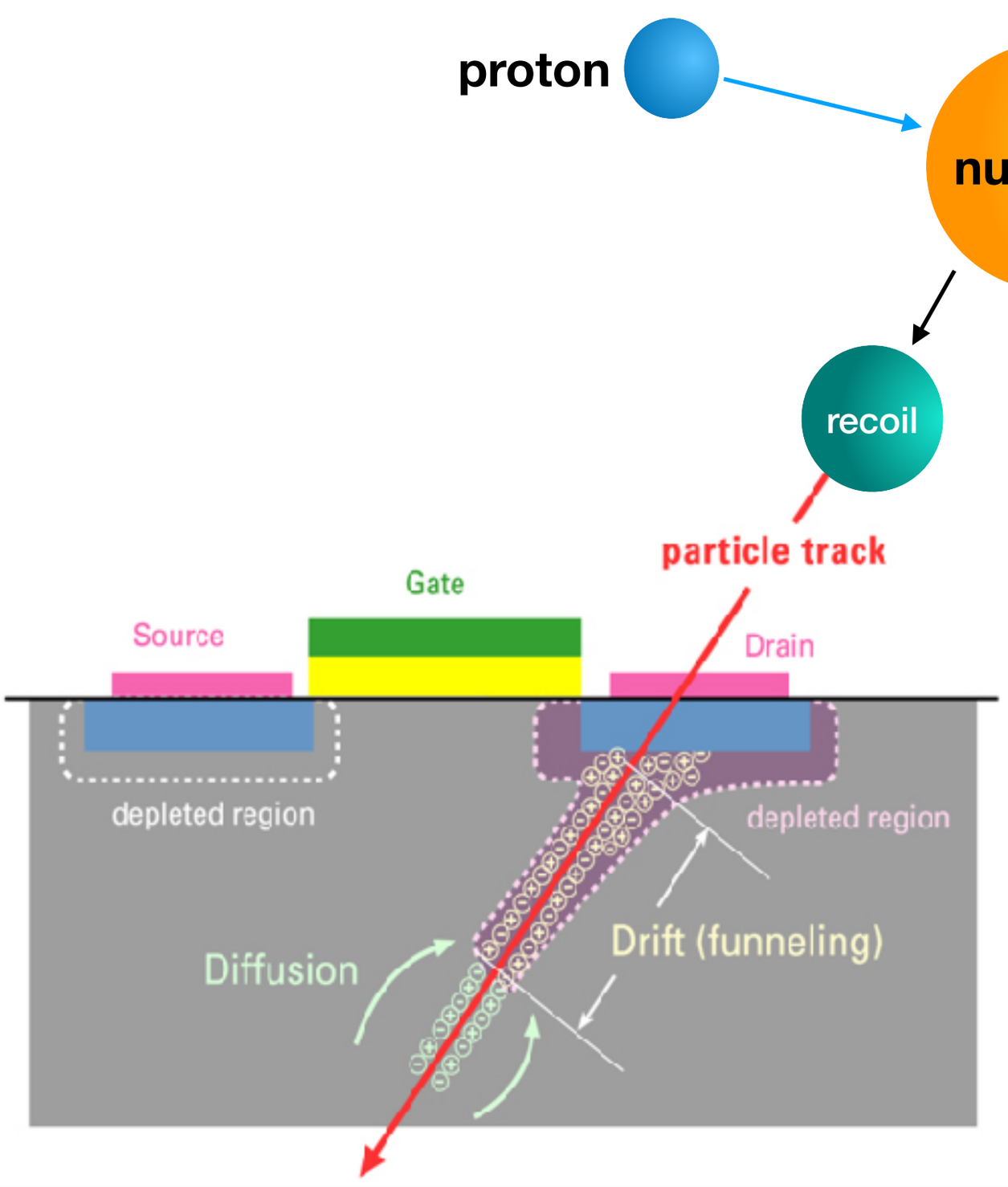


More representative energy range of protons

Energy loss in Silicon



When a recoil with high dE/dx crosses a biased p-n junction, a large amount of charge can be collected rapidly at the electrodes.
These recoils have short range, so they must come from an interaction in proximity of the junction (order of 1-10um for the recoils with high dE/dx)



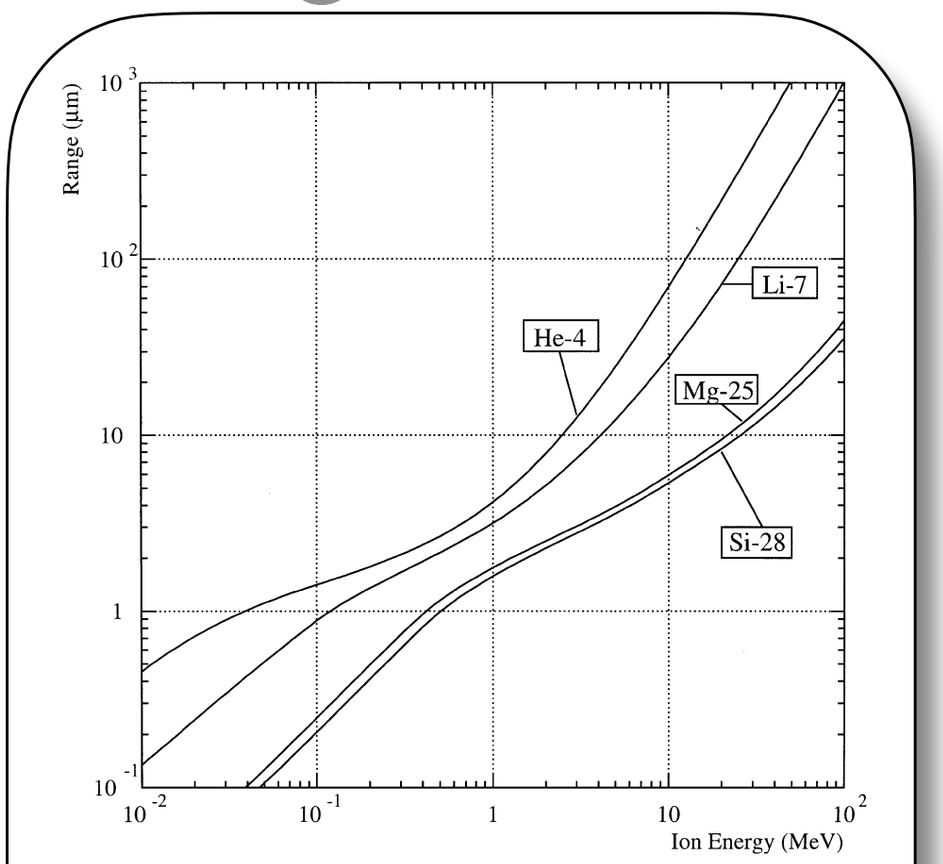
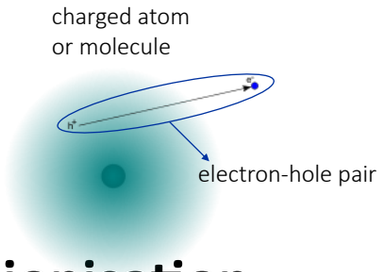


Fig. 2. Ranges of a few ion types in silicon ($\rho = 2.33$ g/cm^3).

after Huhtinen and Faccio, "Computational method to estimate Single Event Upset rates in an accelerator environment", NIM A 450 (2000)

Summary

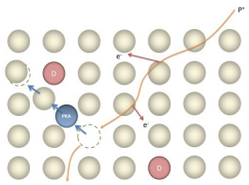


ionisation
(e-h pairs)

if trapped, this charge can **accumulate** in regions of the ICs

Cumulative effects

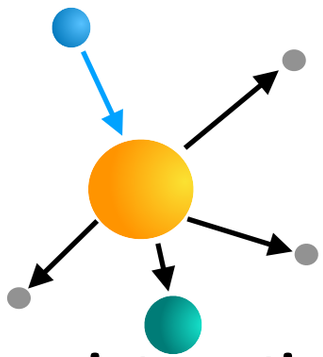
Total Ionising Dose (TID)



non-ionising energy loss (NIEL)

interstitials and vacancies **accumulation**

Displacement Damage (DD)



nuclear interaction
(recoils with large dE/dx)

rapid and intense charge collection in p-n junctions

Single Event Effects (SEE)

Outline

Introduction to ASICs and CMOS technologies

Fundamentals of radiation effects

Radiation effects in CMOS technologies

A brief history of radiation-tolerant ASIC development for LHC

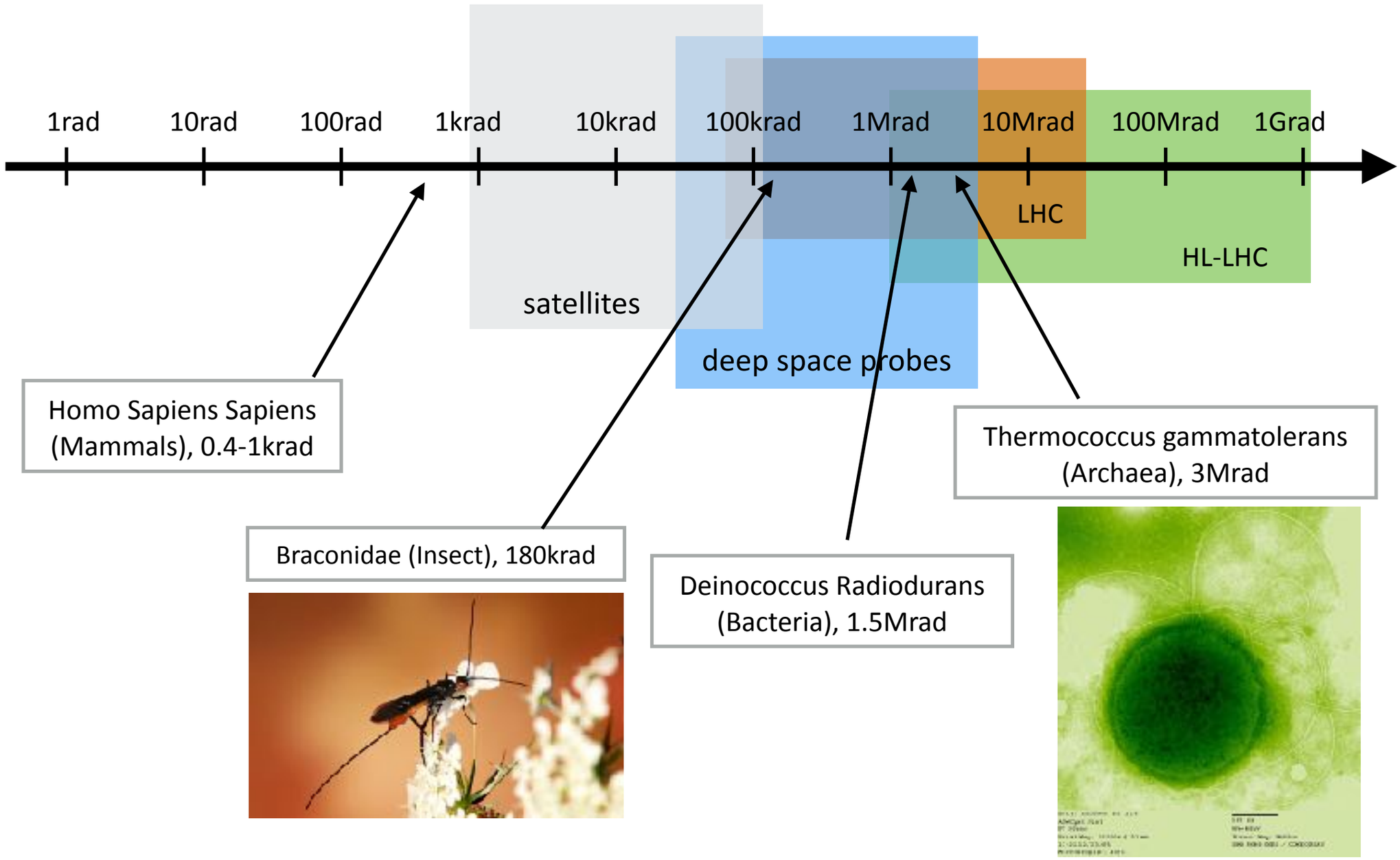
- The first generation of LHC experiments: 0.25µm CMOS
- 130nm CMOS for the upgrades
- Higher radiation levels for HL-LHC: new effects

Case Studies

Total Ionising Dose (TID) effects are traceable to the ionising energy loss in the material, generally SiO_2

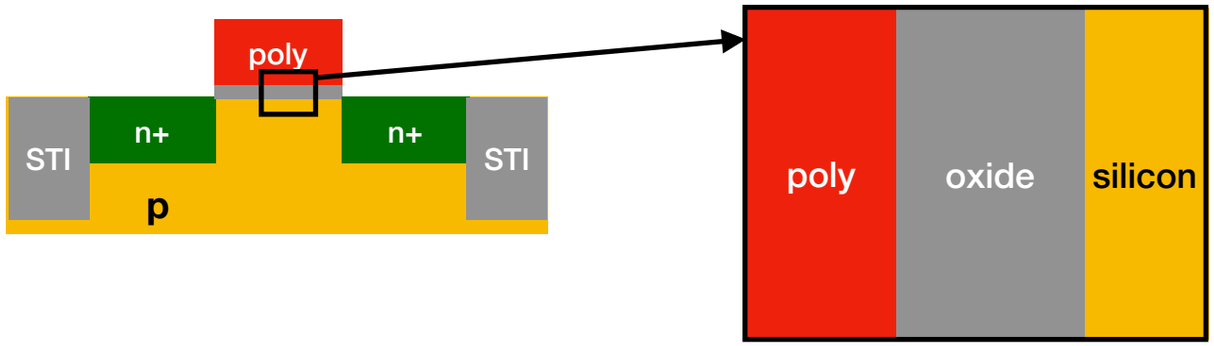
The unit for deposited dose is the Rad

(in the international system it is the Gy, where 1 Gy = 100 rad)

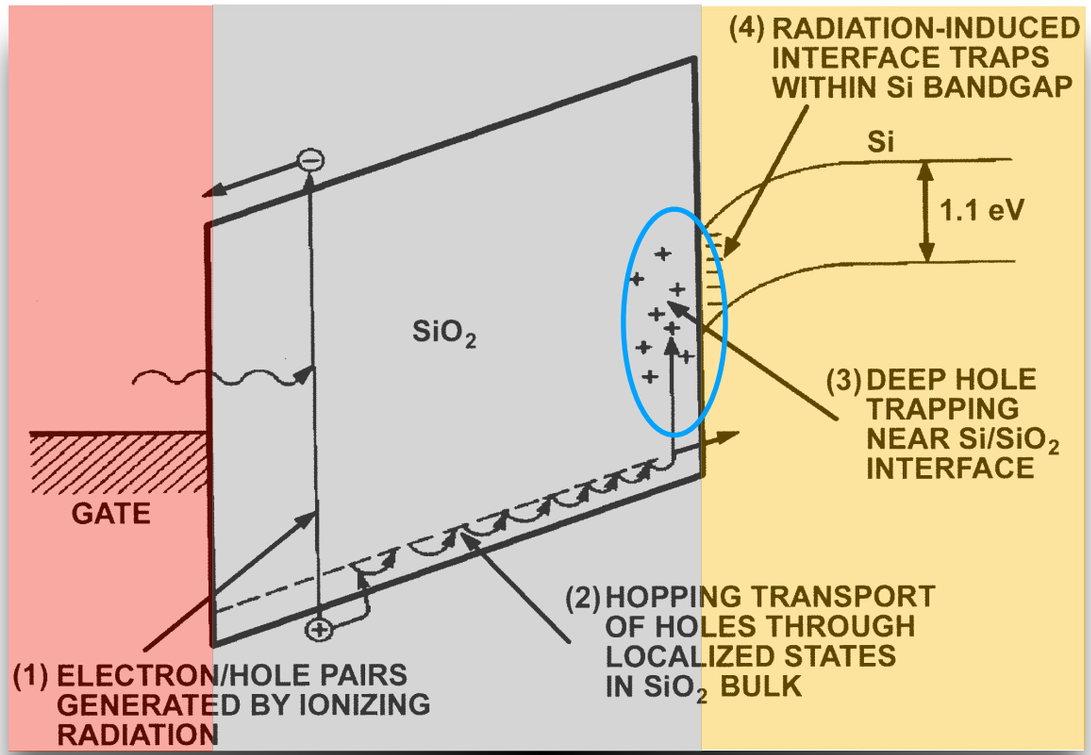


can be killed in 20minutes in our X-ray facility

TID-induced transistor degradation is due to charge trapped in the SiO2 or at its interface with the channel

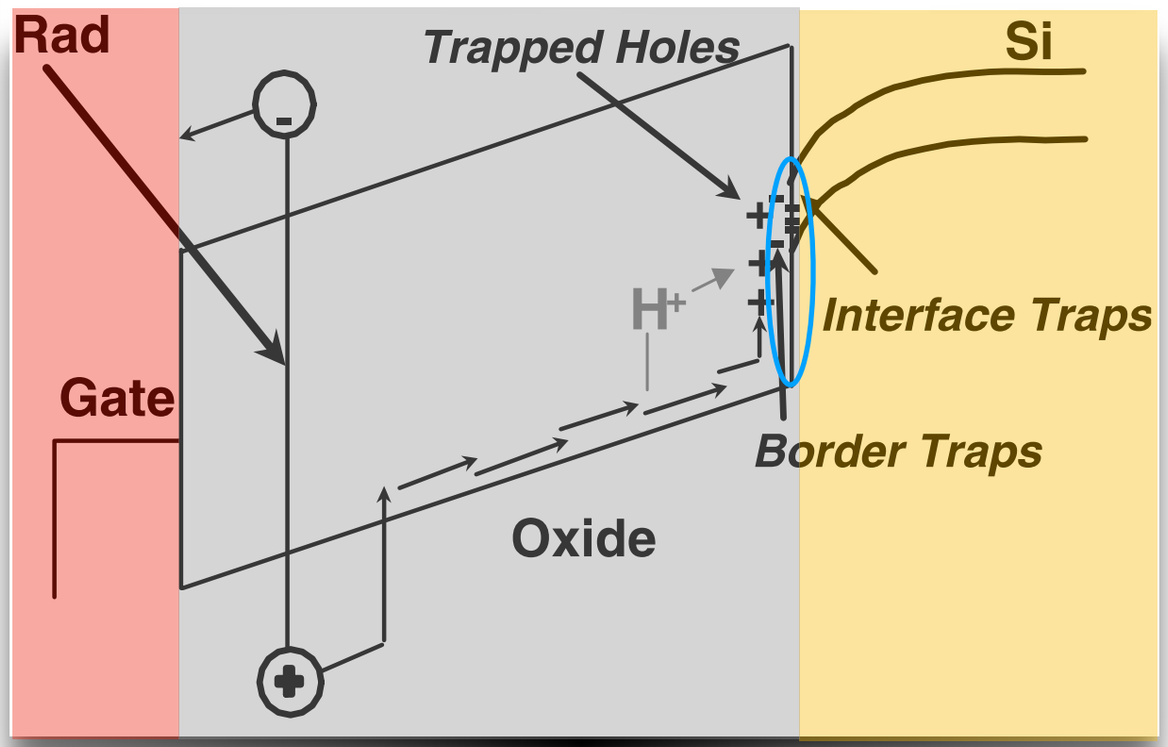


Holes generated by ionisation can be trapped in the oxide ("oxide trapped charge").
The trapped charge is **always POSITIVE**.



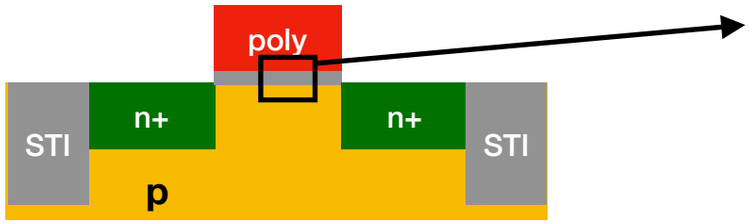
after T.R.Oldham and F.B.McLean, "Total Ionizing Dose Effects in MOS Oxides and Devices", IEEE TNS 50, n.3, 2003

Interface traps require the migration of hydrogen to the interface ("interface states").
The trapped charge depends on the energy at the interface (**NMOS => NEGATIVE, PMOS => POSITIVE**)



after D.M.Fleetwood, "Effects of hydrogen transport and reactions on microelectronics radiation response and reliability ", Microelectronics Reliability 42 (2002) 523–541

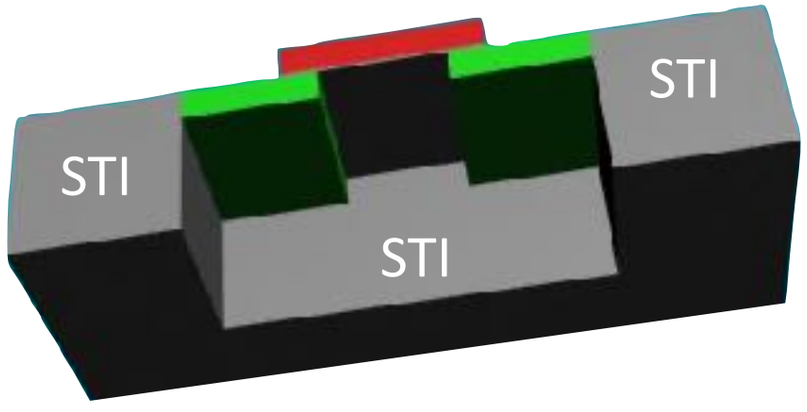
Defects in the gate oxide, in the form of oxide trapped charge and interface traps, influence the characteristics of the transistor

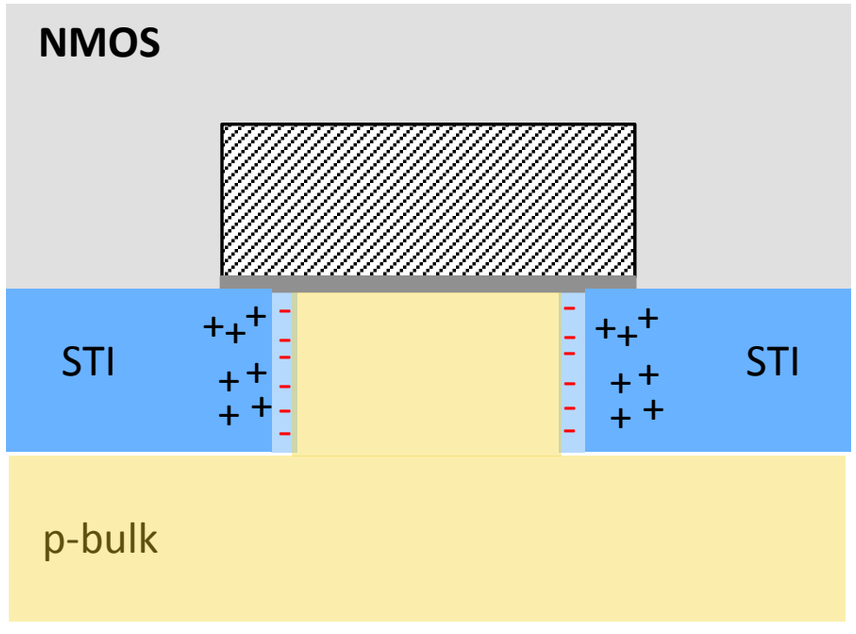


- **Threshold voltage**
- **Transconductance (mobility)**
- **Noise**

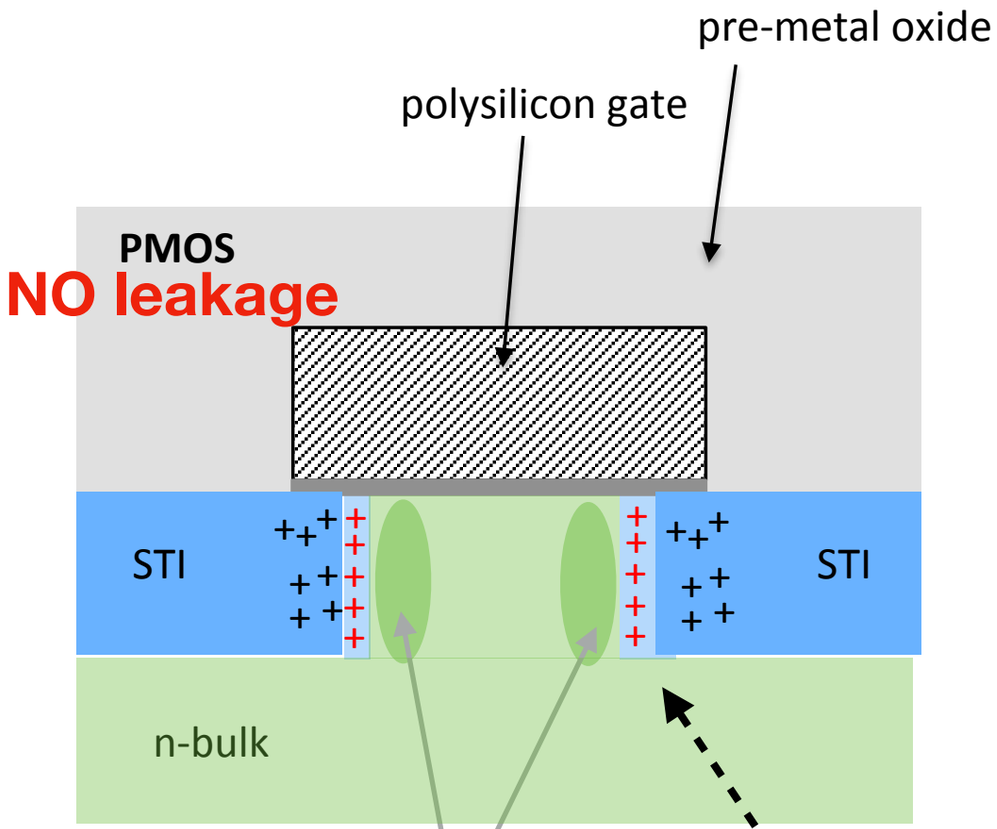
“Negligible” in advanced CMOS

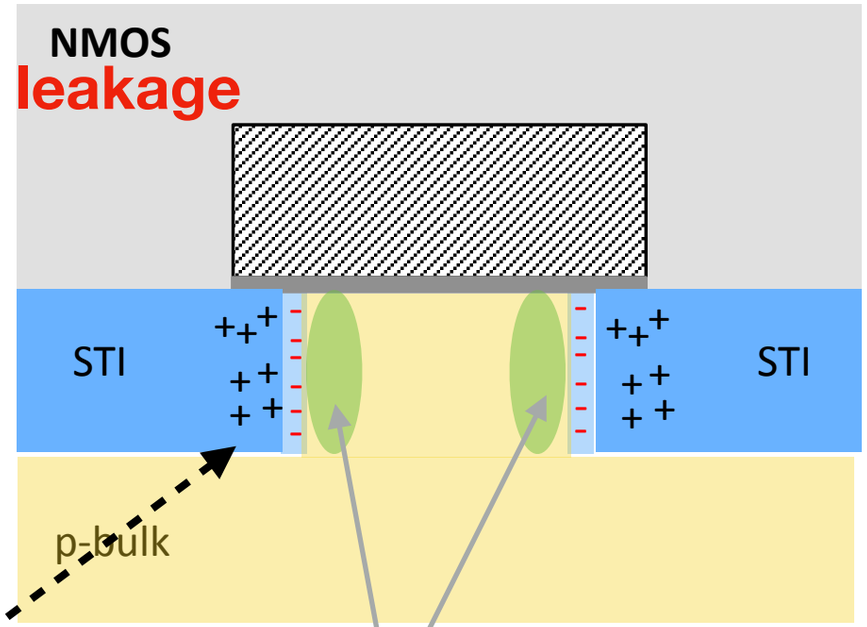
Defects in the field oxide (separation between transistors) might give origin to leakage currents





Defects in the field oxide might give origin to leakage currents
in NMOS transistors only





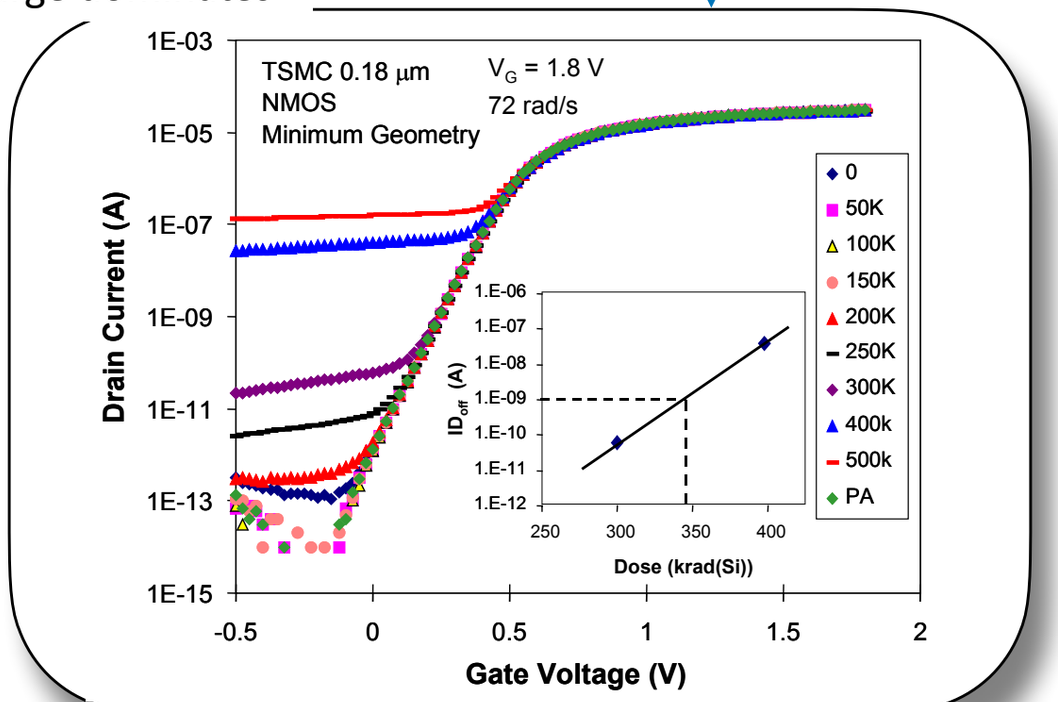
further accumulation

inversion if positive charge dominates

black = “oxide trapped charge”
red = charge in “interface states”

Example

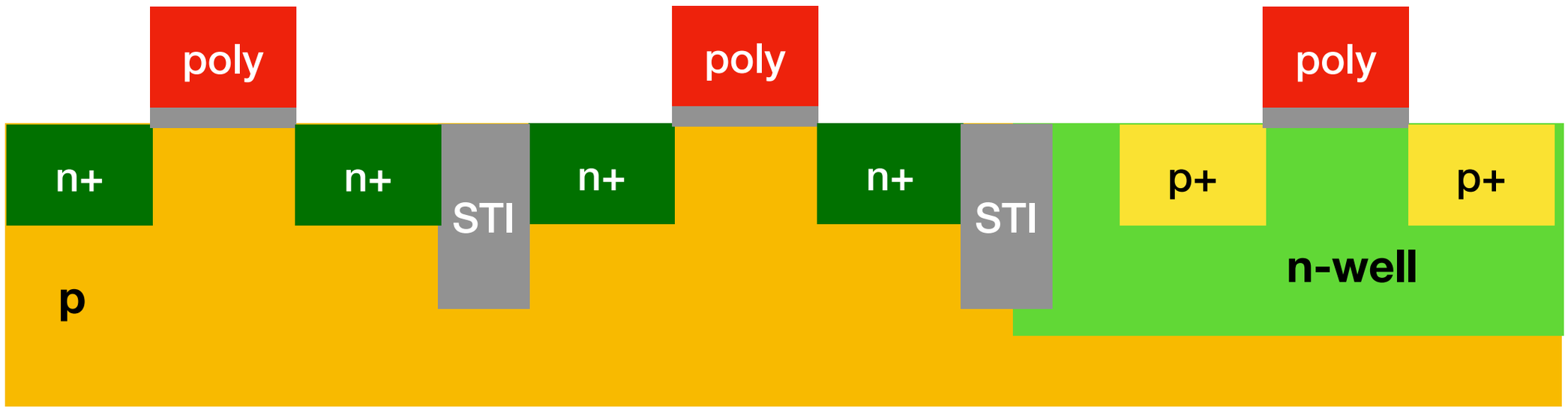
after R.Lacoe, “CMOS scaling, design principles and hardening-by-design methodology”, Short Course at the 2003 NSREC, Monterey



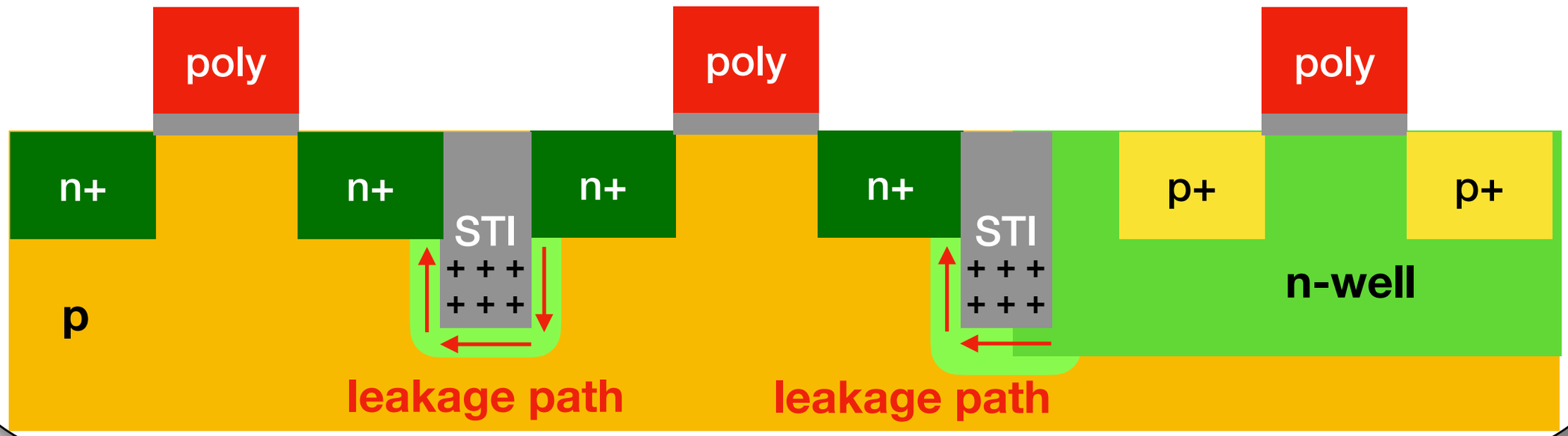
Positive charge trapped in the STI oxide can also open leakage current paths between n+ diffusions at different potential.

Again, this might be mitigated (or suppressed) by negative charge in interface traps.

- **Before irradiation: perfect isolation**



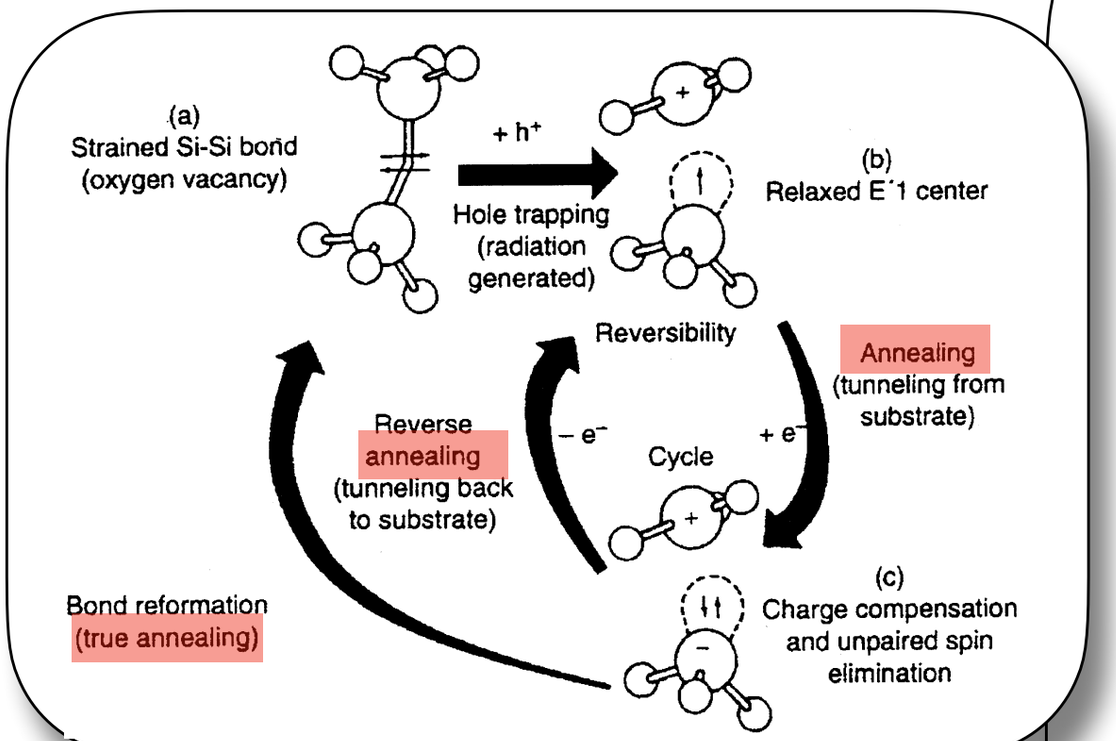
- **After TID accumulation: leakage paths between adjacent transistors and wells**

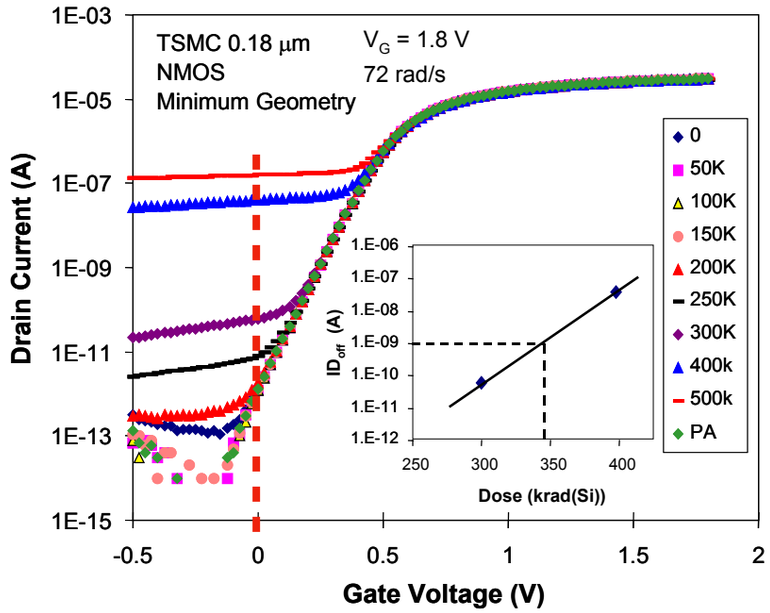


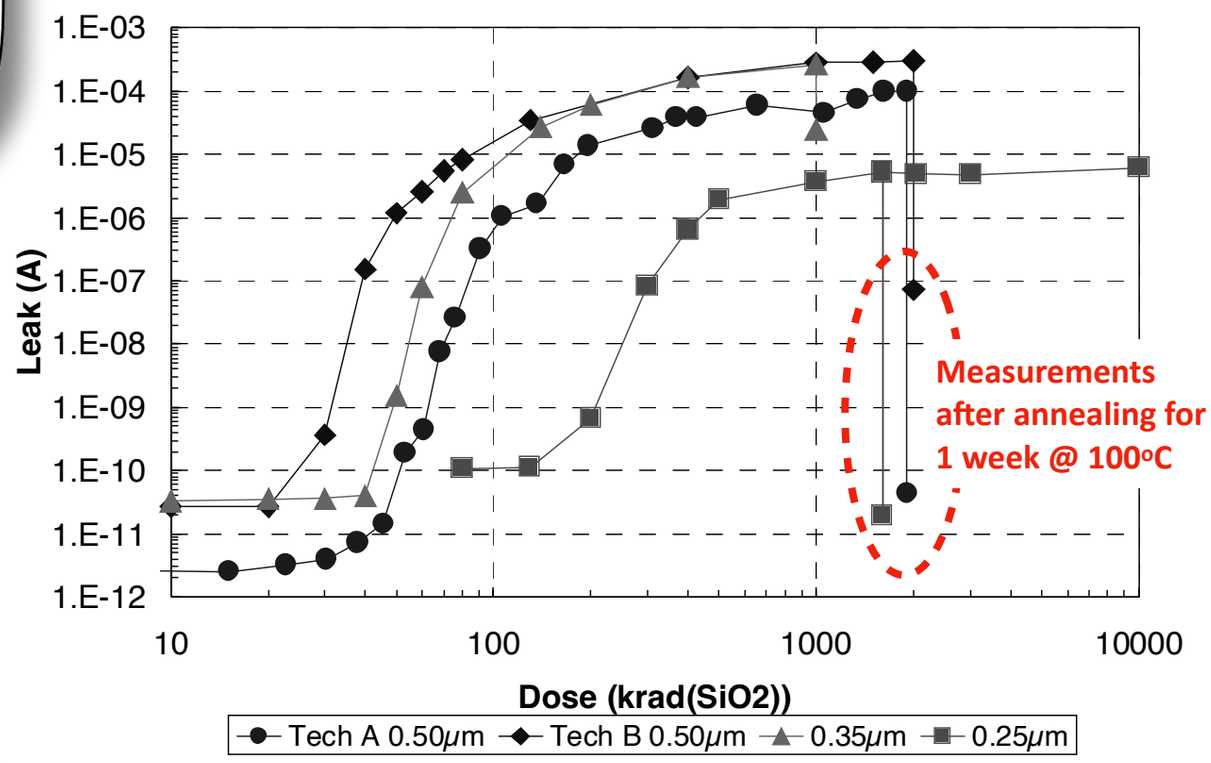
Radiation-induced defects can “anneal”

This is particularly relevant for oxide trapped charge (that induces leakage in NMOS)

The evolution in time depends **on the energy of the trap and on the temperature**







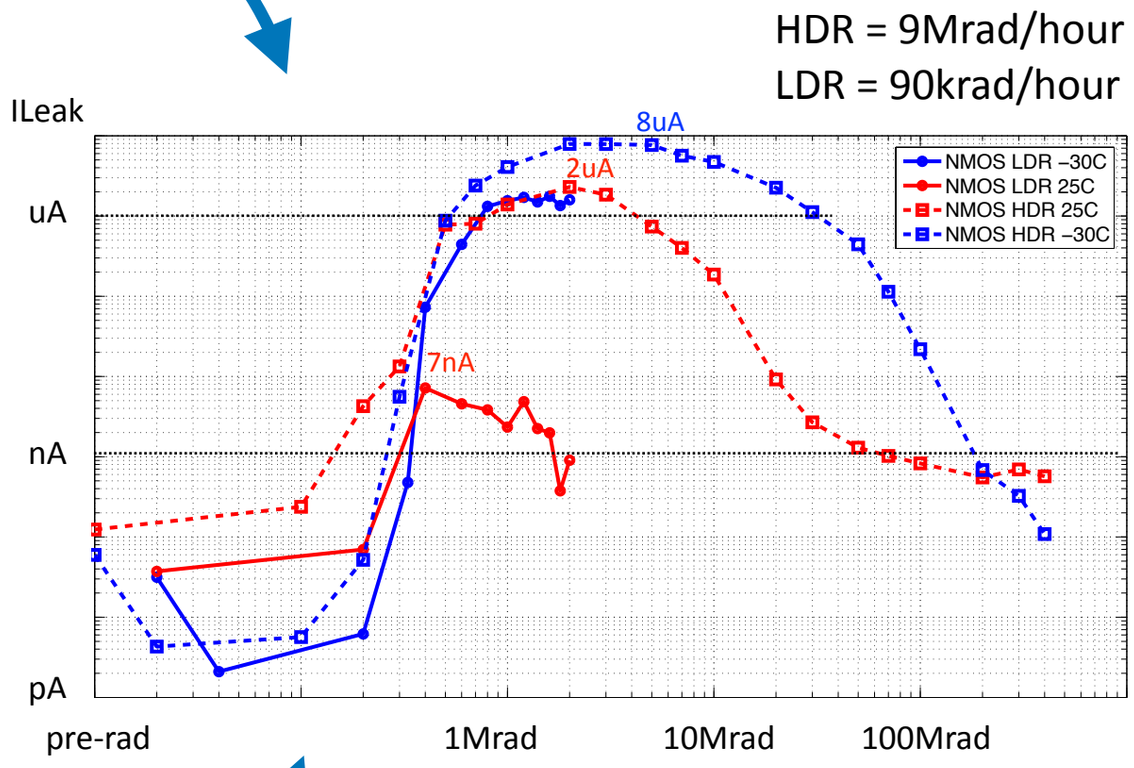
Leakage current: the net result during a test or in the application depends on temperature and dose rate !

Temperature effects

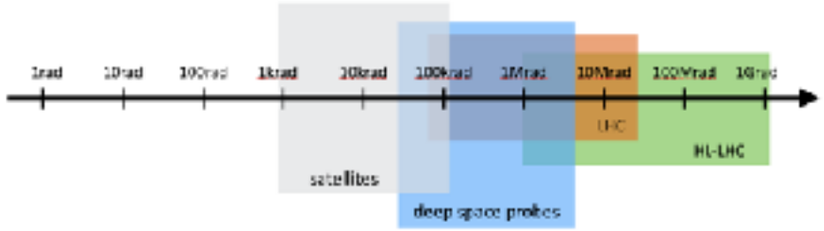
- Hole trapping maximised at low T
- Interface-trap buildup accelerated at higher temperatures (annealing however above 80-125^{o}C)

Dose Rate effects

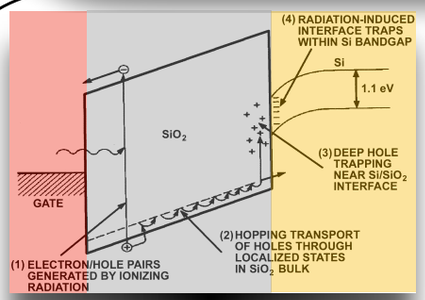
- Hole trapping dominates at high rates and short times
- Interface-trap charge more significant at low rates and long times



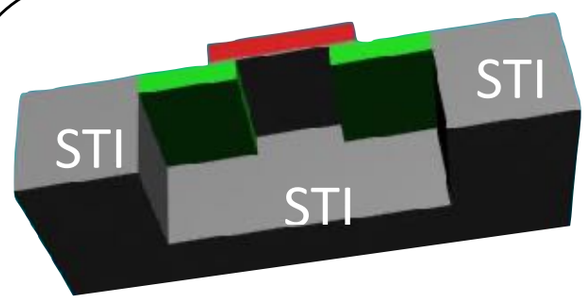
TID (Total Ionising Dose) in CMOS: Summary of Main Concepts



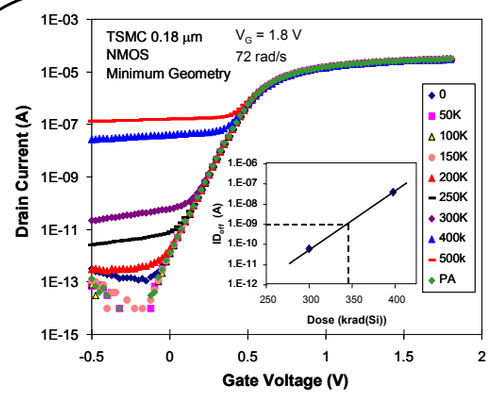
TID levels in HL-LHC experiments are VERY large!

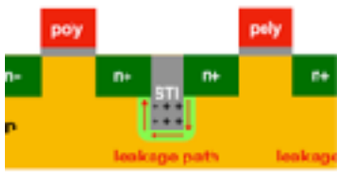


TID effects are due to ionisation in SiO_2

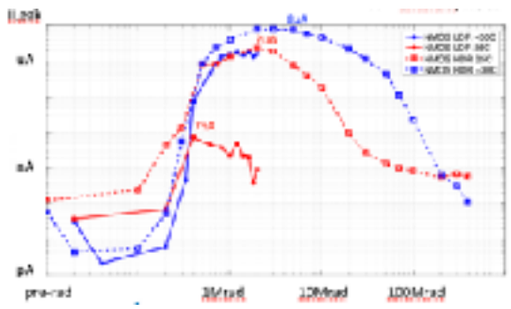


and in advanced CMOS to ionisation in parasitic oxides (STI) rather than in the gate oxide



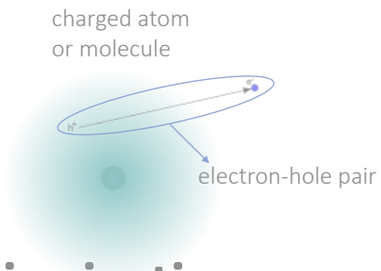


Accumulation of radiation-induced charge in the STI oxide might induce leakage currents in NMOS transistors or between n+ diffusions



The evolution of the leakage depends on dose rate and temperature (and is technology specific)

Summary

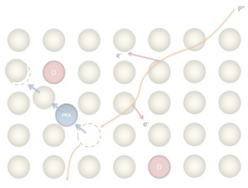


ionisation
(e-h pairs)

if trapped, this charge can **accumulate** in regions of the ICs

Cumulative effects

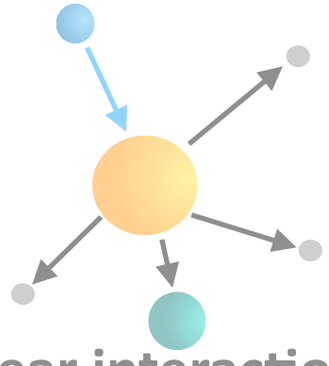
Total Ionising Dose (TID)



non-ionising energy loss (NIEL)

interstitials and vacancies **accumulation**

Displacement Damage (DD)



nuclear interaction
(recoils with large dE/dx)

rapid and intense charge collection in p-n junctions

Single Event Effects (SEE)

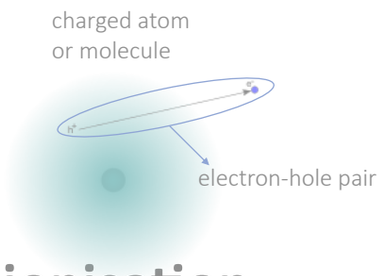
Devices that are affected by displacement damage in CMOS technologies:

- **photodiodes in Active Pixel Sensors**
- **diodes or BJTs used for voltage reference generator circuits**
- **LDMOS (Lateral Diffusion) or Vertical MOS for high-voltage applications**

Recent additional observations (whose generality has to be confirmed):

- leakage current between n-wells in the substrate
- non-applicability of the NIEL scaling for DD

Summary

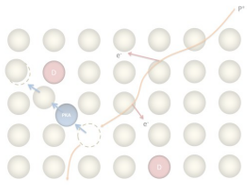


ionisation
(e-h pairs)

if trapped, this charge can **accumulate** in regions of the ICs

Cumulative effects

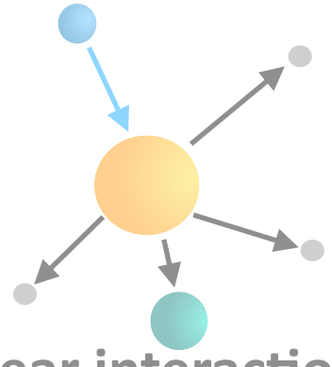
Total Ionising Dose (TID)



non-ionising energy loss (NIEL)

interstitials and vacancies **accumulation**

Displacement Damage (DD)

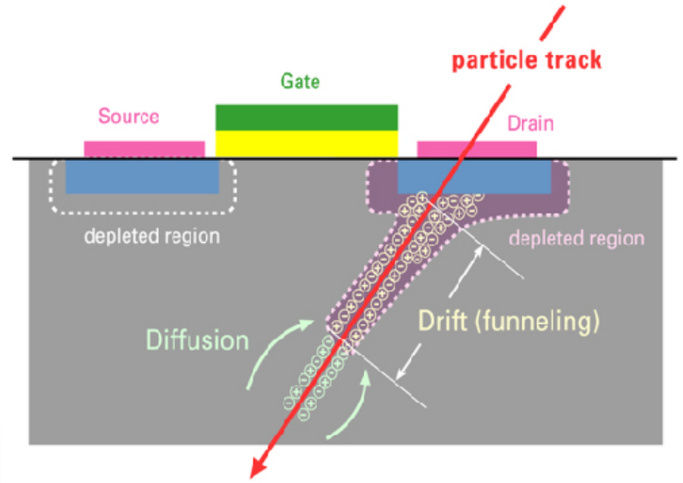


nuclear interaction
(recoils with large dE/dx)

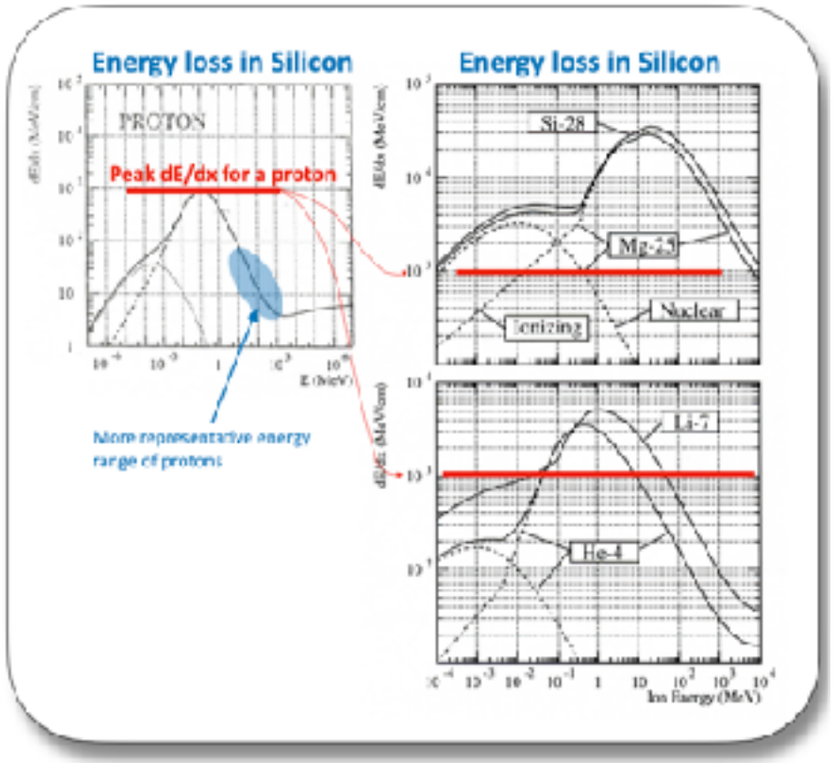
rapid and intense charge collection in p-n junctions

Single Event Effects (SEE)

Single Event Effects are due to the instantaneous and local deposition of ionising energy from a single particle



BUT **the dE/dx should be sufficiently large** for the deposition of charge exceeding a “threshold”.
Typically for CMOS the threshold is above the dE/dx of protons

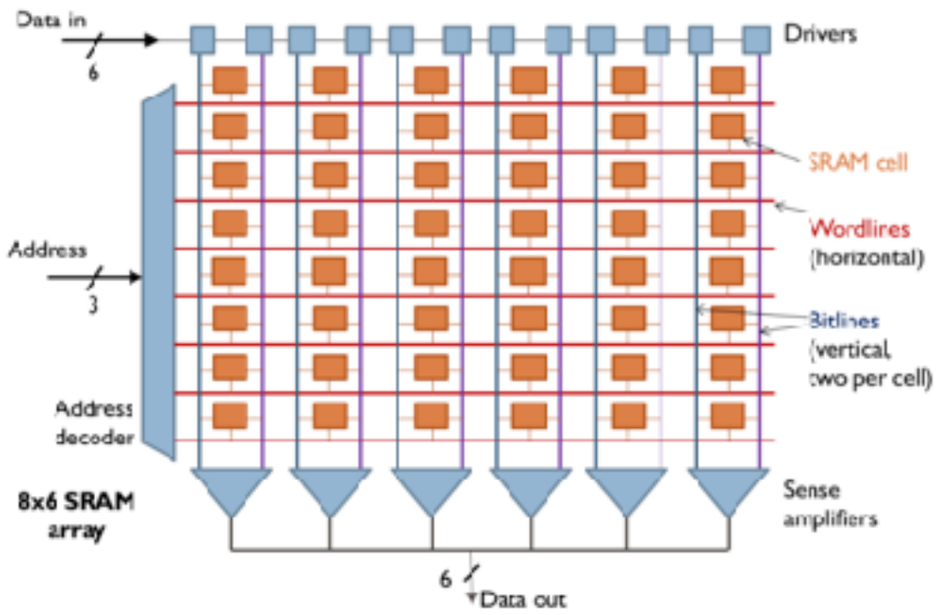


If the deposited charge is sufficient, in CMOS:

Single Event Upset (SEU)
Single Event Transient (SET)
Single Event Latch-up (SEL)

Single Event Upset (SEU): corruption of one bit in a register or memory cell

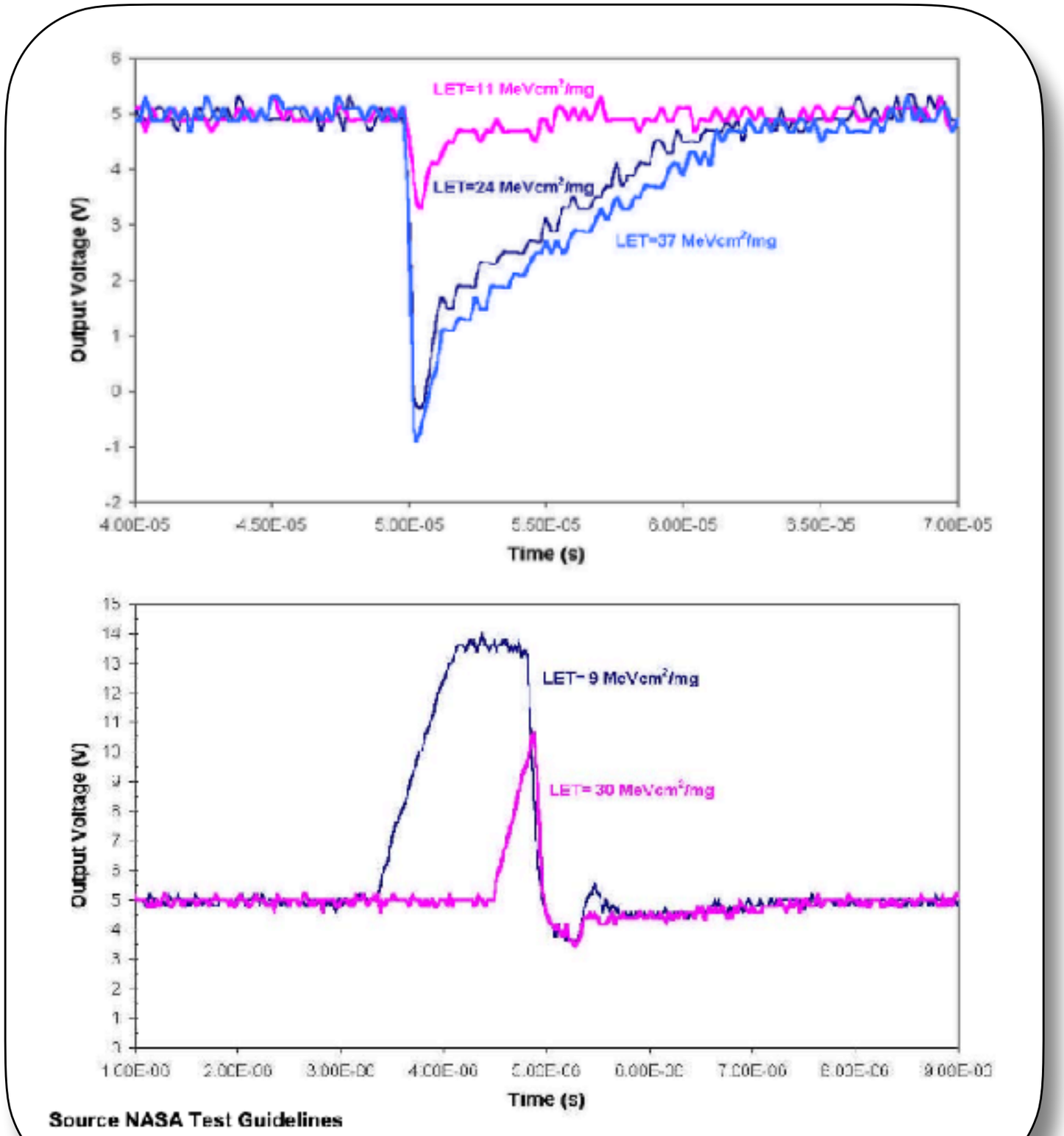
10011001



10010001

Possible consequences

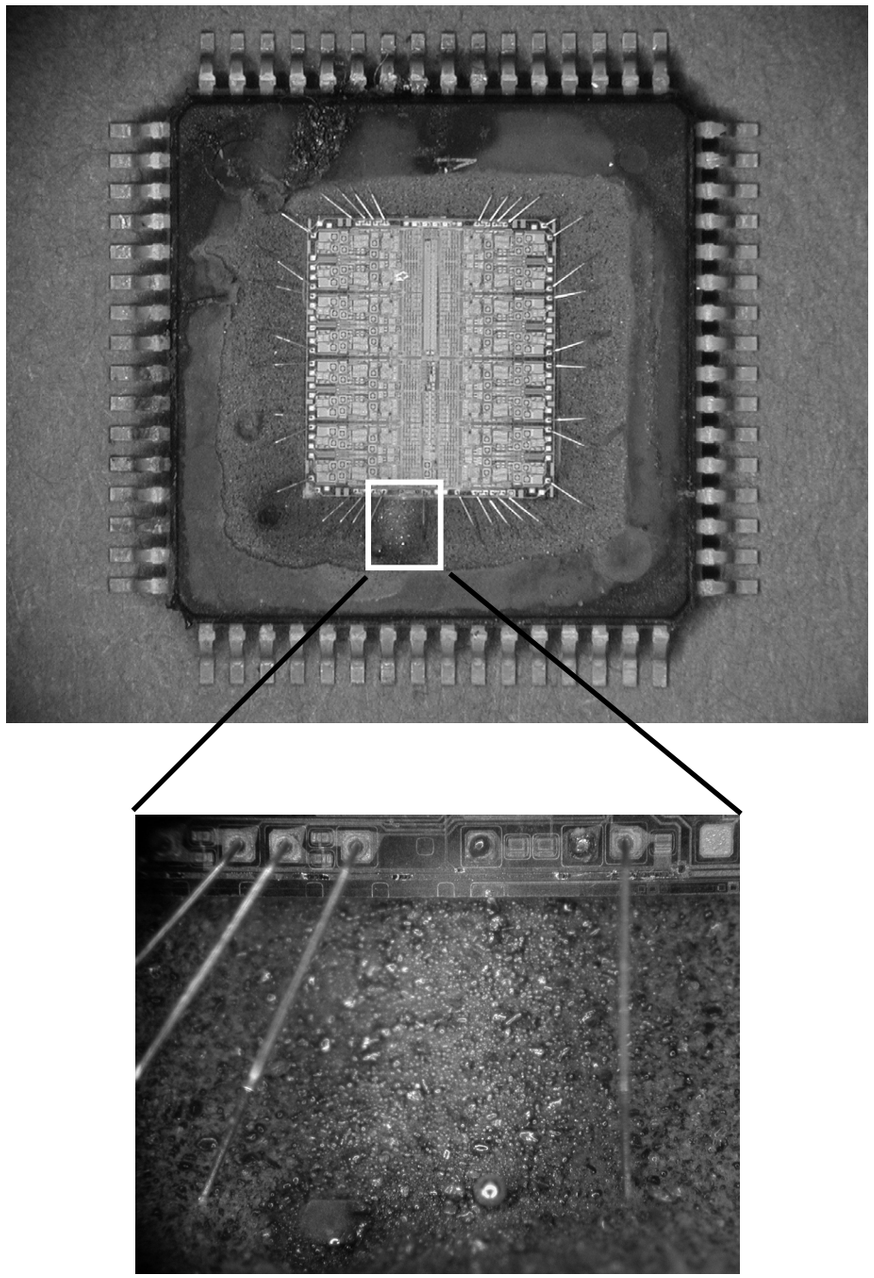
Single Event Transient (SET): current/voltage pulse that can propagate in the circuit



Source NASA Test Guidelines

Single Event Latch-up (SEL): turn-on of a parasitic thyristor structure

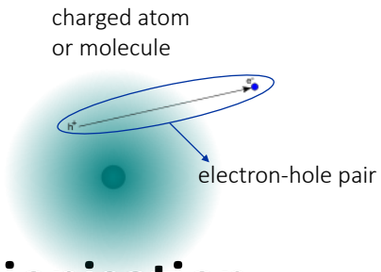
Latch-up might lead to permanent device damage



Single Event Latchup (SEL) of a high voltage driver for MEMS (vaporized bond wires)

After M.O'Bryan et al., "Current Single Event Effects and Radiation Damage Results for Candidate Spacecraft Electronics", NSREC Radiation Effects Data Workshop 2002

Summary

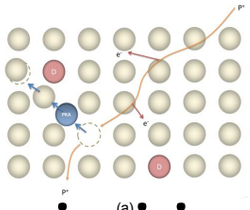


ionisation
(e-h pairs)

Cumulative effects

Total Ionising Dose (TID)

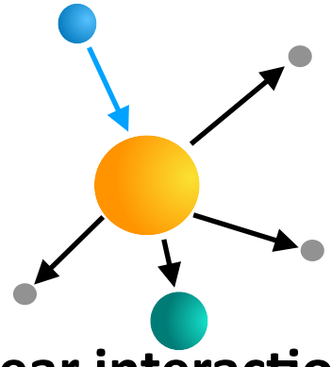
Can be addressed by technology or by design



non-ionising energy loss (NIEL)

Displacement Damage (DD)

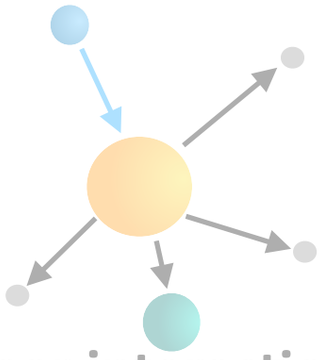
Generally not significant in CMOS



nuclear interaction
(recoils with large dE/dx)

Single Event Effects (SEE)

Always need design countermeasures



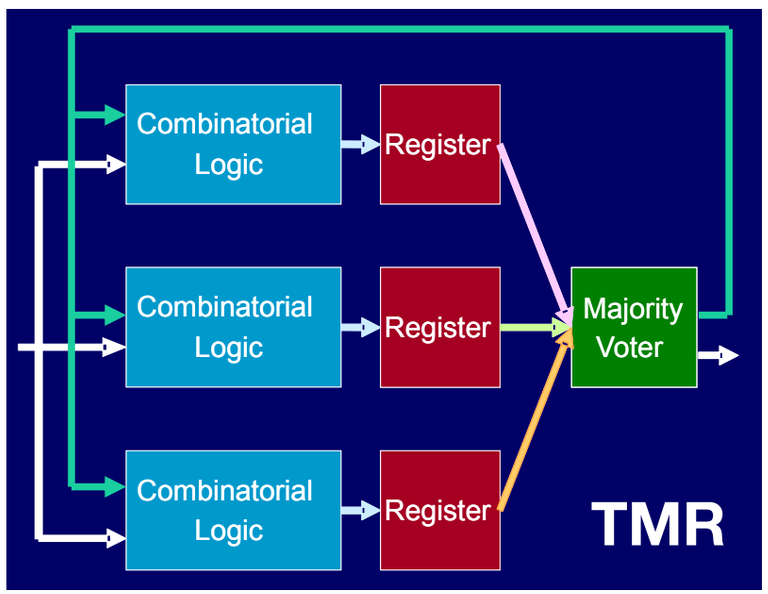
nuclear interaction
(recoils with large dE/dx)

Single Event Effects (SEE)

Always need design countermeasures

Upset, Transient (SEU, SET)

- Add redundancy
  - TMR (Triplication)
  - Encoding
- For SET, add filtering



Latch-up (SEL)

- Technology dependent
- Reduce distance between substrate contacts
- Insert guard-rings

Outline

Introduction to ASICs and CMOS technologies

Fundamentals of radiation effects

Radiation effects in CMOS technologies

A brief history of radiation-tolerant ASIC development for LHC

The first generation of LHC experiments: 0.25µm CMOS

130nm CMOS for the upgrades

Higher radiation levels for HL-LHC: new effects

Case Studies

Radiation-hard ASICs for the development of LHC electronics (ca. 1990-2000)

- Dedicated Rad-Hard processes quickly ruled out (only DMILL used in LHC experiments)

ELSEVIER

Nuclear Instruments and Methods in Physics Research A 399 (1997) 129–139

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

Radiation hardened transistor characteristics for applications at LHC and beyond

M. Millmore[a,*], M. French[b], G. Hall[a], M. Raymond[a], G.F[illegible]

[a] *Imperial College, London, SW7 2BZ, UK*
[b] *Rutherford Appleton Laboratory, Didcot, Chilton, Oxo[illegible]*

Received 10 June 19[illegible]

HARRIS 1.2um bulk technology

Abstract

The high-radiation environment at the LHC will requir[illegible] use of radiation-hardened microelectronics for the read out of inner detectors. Ty[illegible] Transistors have been [illegible] expected in the innerr[illegible] samples from one hav[illegible] microstrip tracker, has[illegible]

PACS: 61.80E; 61.82[illegible]
Keywords: Radiation-[illegible]

CERN LIBRARIES, GENEVA

SC00000136

CERN/DRDC/92-31
DRDC/P42
14 May 1992

R&D Proposal

A Mixed Analog-Digital Radiation Hard Technology for High Energy Physics Electronics:

DMILL (Durci Mixte sur Isolant Logico-Linéaire)

Spokesman : M.Dentan (Technolo[illegible]
Co-spokesman : E. Beuville [illegible]

E.Beuville, P.Borgeaud, M[illegible], M.Rouger
CEA-DSM-DAPNIA Saclay [illegible]ette, France.

J.P.Blanc, M.Bruel, E.Del[illegible]ier, J. de Pontcharra, R.Truche
CEA-[illegible] Grenoble, France.

E.Du[illegible]t, J.L.Leray, J.L.Martin, J.Montaron
CEA-Cen[illegible]res le Châtel, F-91680 Bruyères-le-Châtel, France.

[illegible]borel, J.M.Brice, P.Chatagnon, C.Terrier
Thomson TMS, F-38521 Grenoble, France.

J.J.Aubert, P.Delpierre, M.C.Habrard, R.Potheau
IN2P3-CPPM, F-13288 Marseille, France.

DMILL 0.8um SOI technology

ELSEVIER

Nuclear Physics B (Proc. Suppl.) 78 (1999) 708–712

NUCLEAR PHYSICS B PROCEEDINGS SUPPLEMENTS
www.elsevier.nl/locate/npe

Performance of Honeywell RICMOS-IV SOI Transistors After Irradiation to 27 Mrad(Si) by 63.3 MeV Protons *

D.E. Pellett[1] and S.T. Liu[2]
[1]Physics Department, UC Davis, Davis, CA 95616
[2]Honeywell Solid State Electronics Center, Minneapolis, Minnesota 5[illegible]

We present results of an exposure of Honeywell RICMOS-IV [illegible]oduced in a developmental run to 2×10^{14} 63.3 MeV protons at the UCD cyclotron rad[illegible] [illegible]27 Mrad (Si)). In terms of surface damage, this corresponds to almost twice the dose e[illegible]MS pixel detector during its useful life at the LHC collider. The irradiated transistors incl[illegible]OSFETs similar to the front-end transistors of a pixel readout suitable for use at hadron collid[illegible]esented for MOSFETs on radiation-induced changes in thresholds, transconductance, maximum vo[illegible] and noise. Circuit simulations using the measured noise data indicate that the pixel readout would conti[illegible]e to function satisfactorily in the CMS radiation environment.

Honeywell 0.8um SOI technology

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 39, NO. 6, DECEMBER 1992 1739

Study of device parameters for analog IC design in a 1.2μm CMOS-SOI technology after 10 Mrad. *

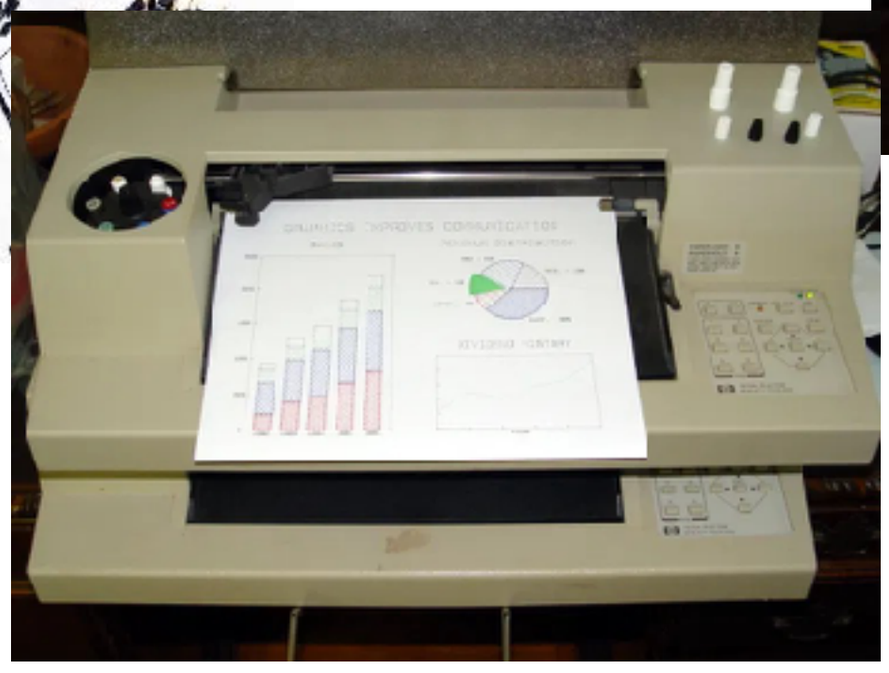
F.Faccio, E.H.M.Heijne, P.Jarron, M.Glaser, G.Rossi, S[illegible]
CERN, 1211 Geneva 23, Switzerland
G.Borel
THOMSON TMS, Avenue de Rochepla[illegible] France

Thomson TCS 1.2um SOI technology

Studying radiation tolerance with the tools of the 90s

Irradiation:
- TID @ CEA Saclay, Pagure
- Neutrons @ CERN PS-ACOL (neutrons from antiproton production target, 3e14 over 2 months)

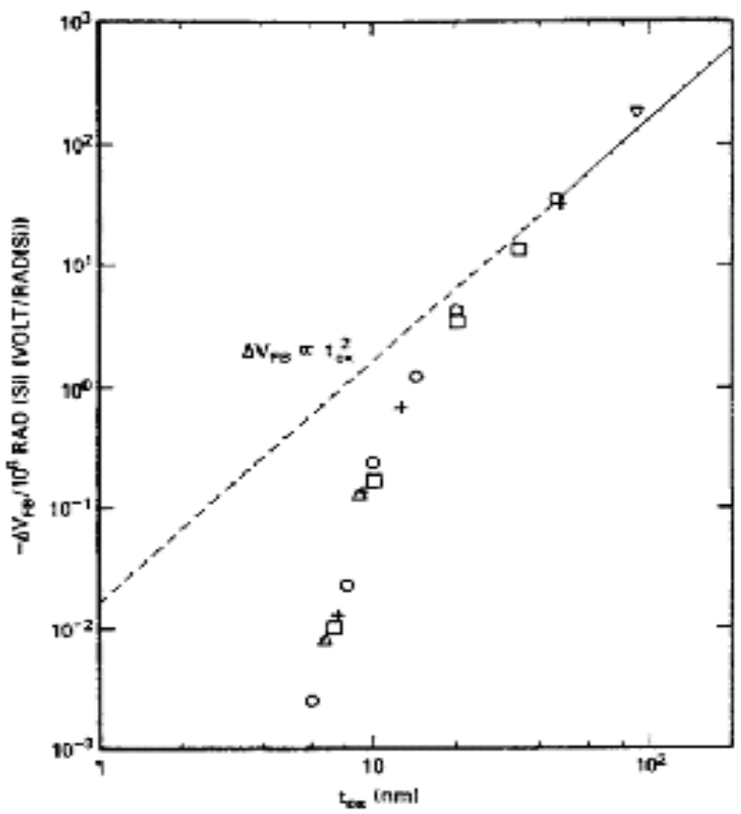
Measurements:
- Chips packaged in DIL
- Individual transistors manually connected sequentially
- Data saved on floppy disks
- Curves plotted with pencil plotter and interpolated manually to extract the parameters



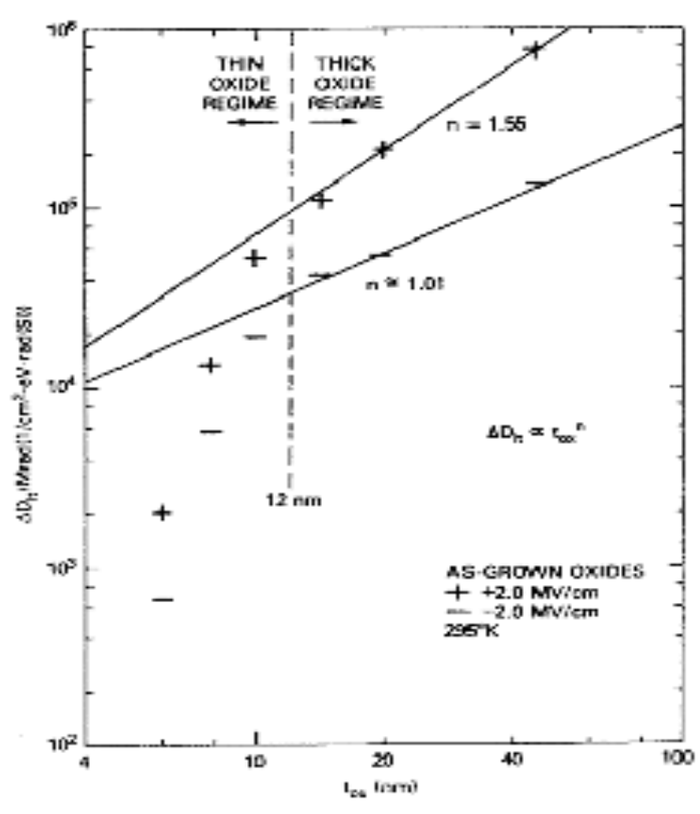
Radiation-hard ASICs for the development of LHC electronics (ca. 1990-2000)

- With gate oxides getting thinner than 5-6nm, they became naturally “radiation tolerant” to very high doses

Oxide trapped charge



Interface states



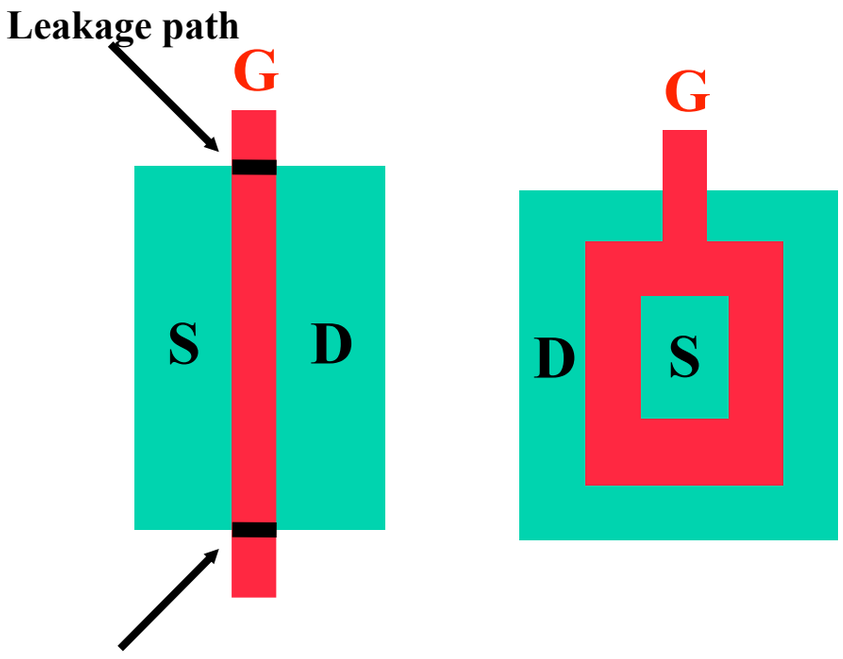
N.S. Saks et al., IEEE TNS, Dec. 1984 and Dec. 1986

Radiation-hard ASICs for the development of LHC electronics (ca. 1990-2000)

- With gate oxides getting thinner than 5-6nm, they became naturally “radiation tolerant” to very high doses
  - parasitic oxides (mainly STI) are the main limit to the radiation tolerance
  - with the systematic adoption of Hardness-By-Design (HBD) techniques, it is possible to avoid STI-related damage

Thin gate oxide + HBD techniques = Radiation tolerance

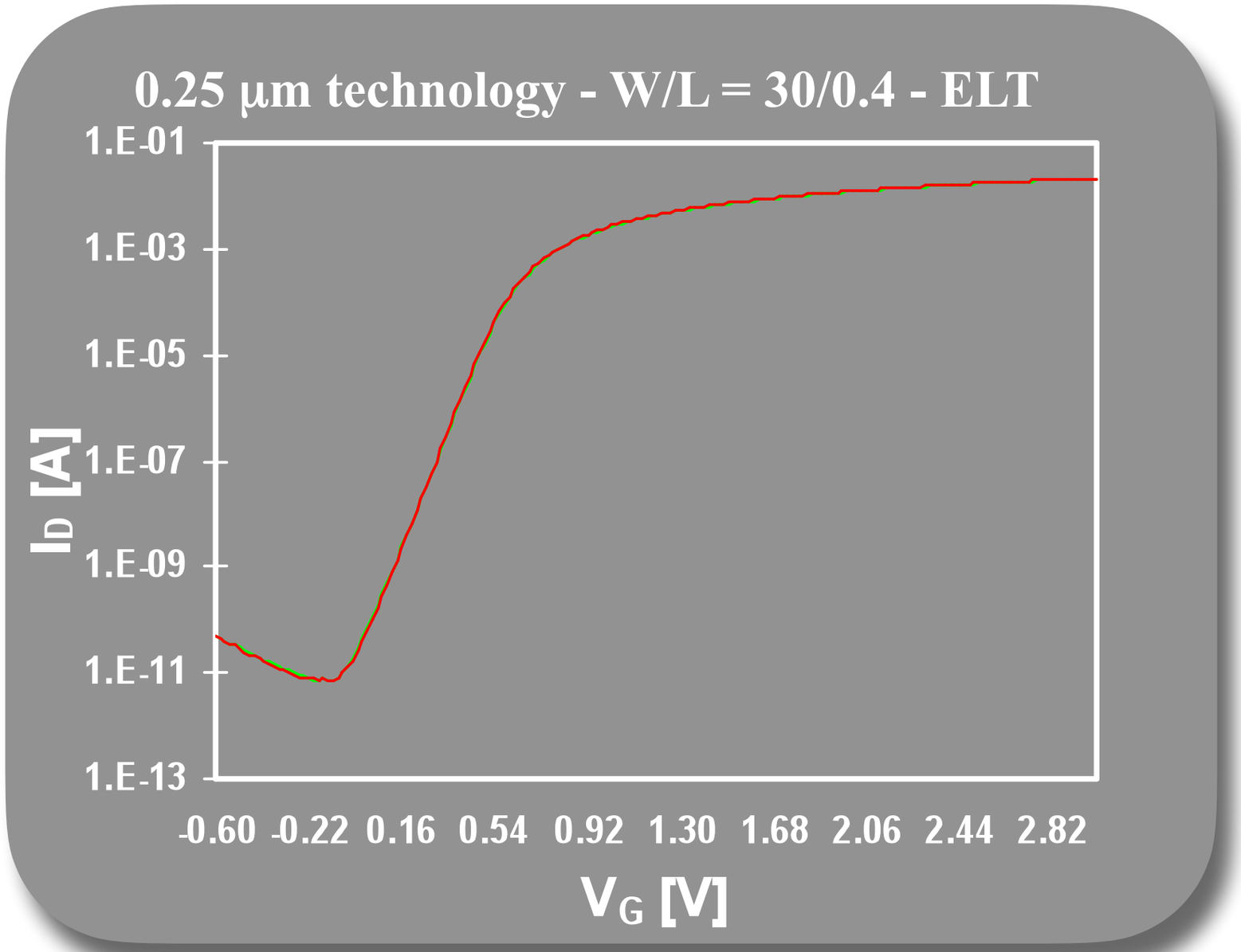
Enclosed Layout Transistors (ELT)



&

Guard-rings

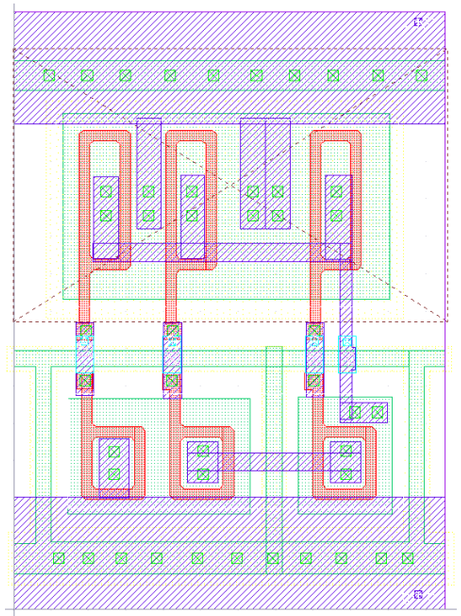
ELT transistors in 0.25um technology: no relevant TID effects up to 10Mrad



Id=f(Vg) pre- and post- 13Mrad

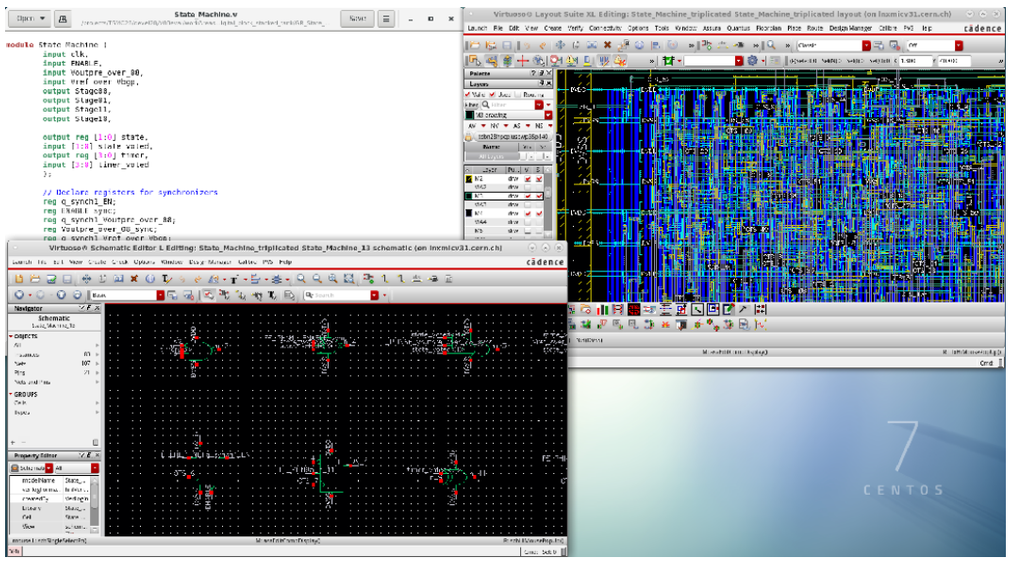
Radiation-hard ASICs for the development of LHC electronics (ca. 1990-2000)

Enclosed Layout Transistors (ELT) + Guard-rings

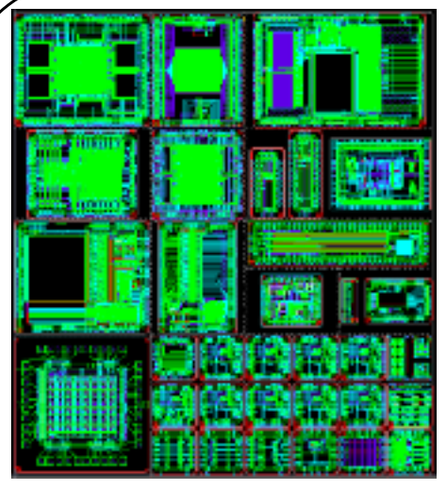


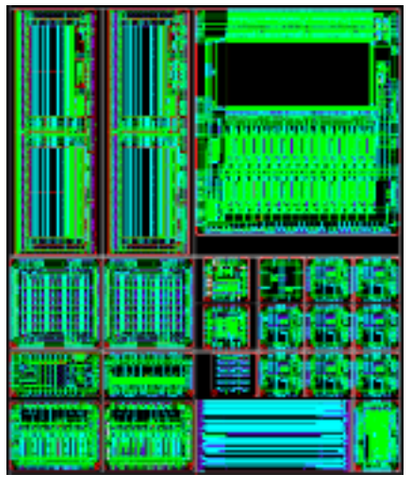
Most of the ASICs used today in LHC experiments are designed using these techniques in a 250nm CMOS process

This required the development of a dedicated “library” of cells with ELT transistors

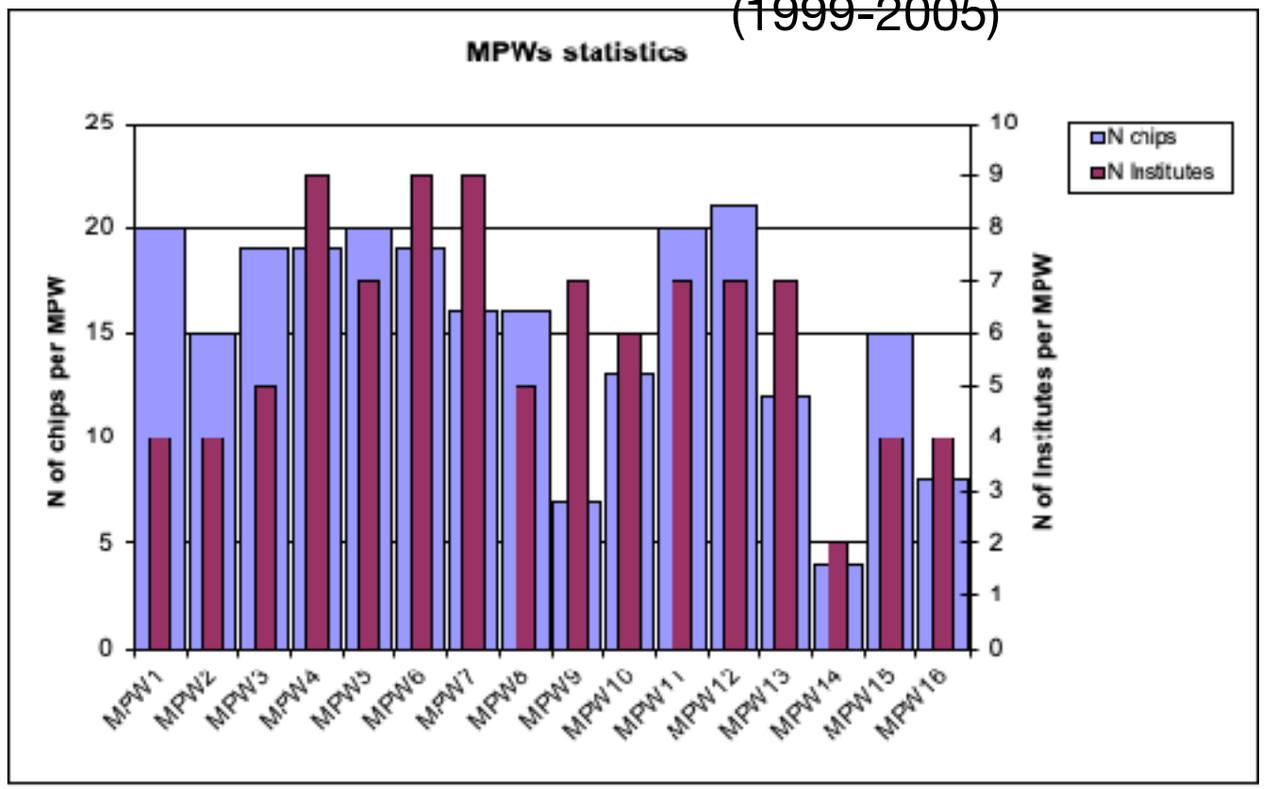


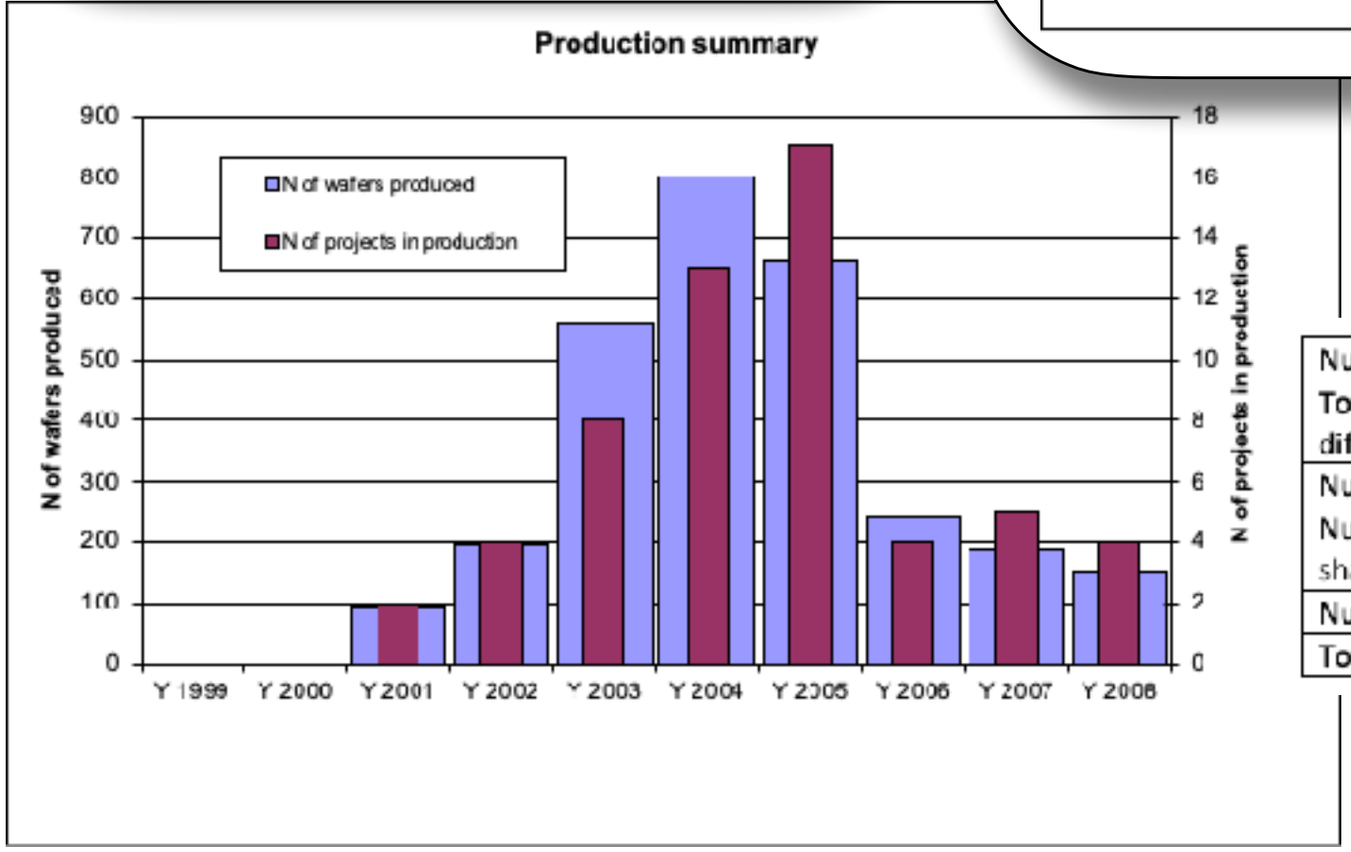
The CERN “Foundry Service”





(1999-2005)





Number of MPW runs	16
Total number of ASICs in MPWs (evolutions of the same ASIC on different MPW runs are re-counted)	244
Number of Institutes participating in MPWs	20
Number of dedicated Mask Sets (full Engineering runs; many are shared between different ASICs)	24
Number of wafers produced	3100
Total expenditure for all the above	13.3MChF

Radiation hard processes

Hardness By Design (HBD) in commercial-grade processes

Production for LHC:
0.25um CMOS

ca. 1998-2000

time

TID up to 10Mrad

TID

Main transistor

V_{th}, g_m, …

Leakage in parasitics

Leakage in parasitics

Outline

Introduction to ASICs and CMOS technologies

Fundamentals of radiation effects

Radiation effects in CMOS technologies

A brief history of radiation-tolerant ASIC development for LHC

The first generation of LHC experiments: 0.25µm CMOS

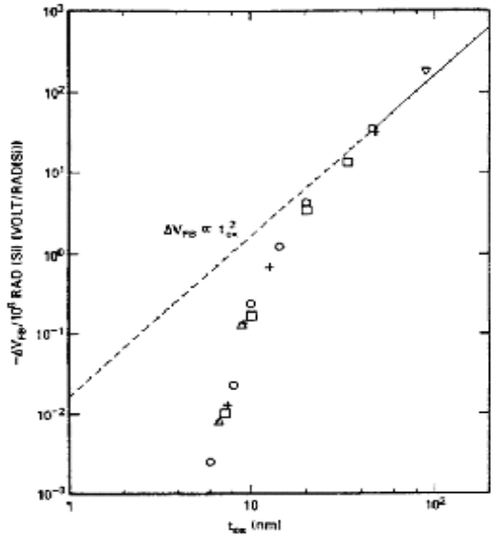
130nm CMOS for the upgrades

Higher radiation levels for HL-LHC: new effects

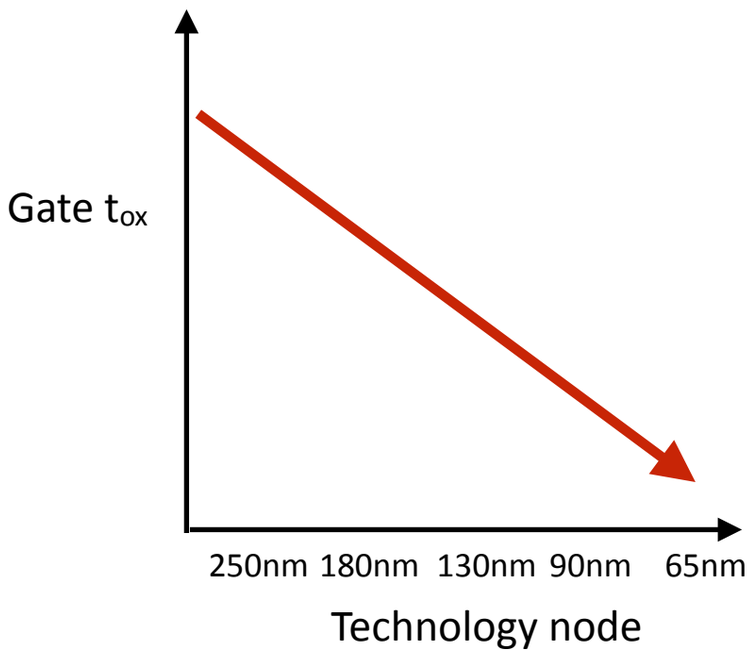
Case Studies

Is this extrapolation correct?

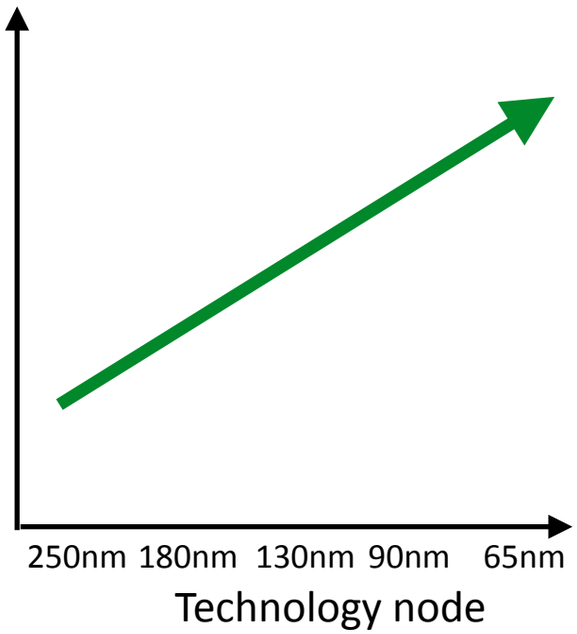
TID damage

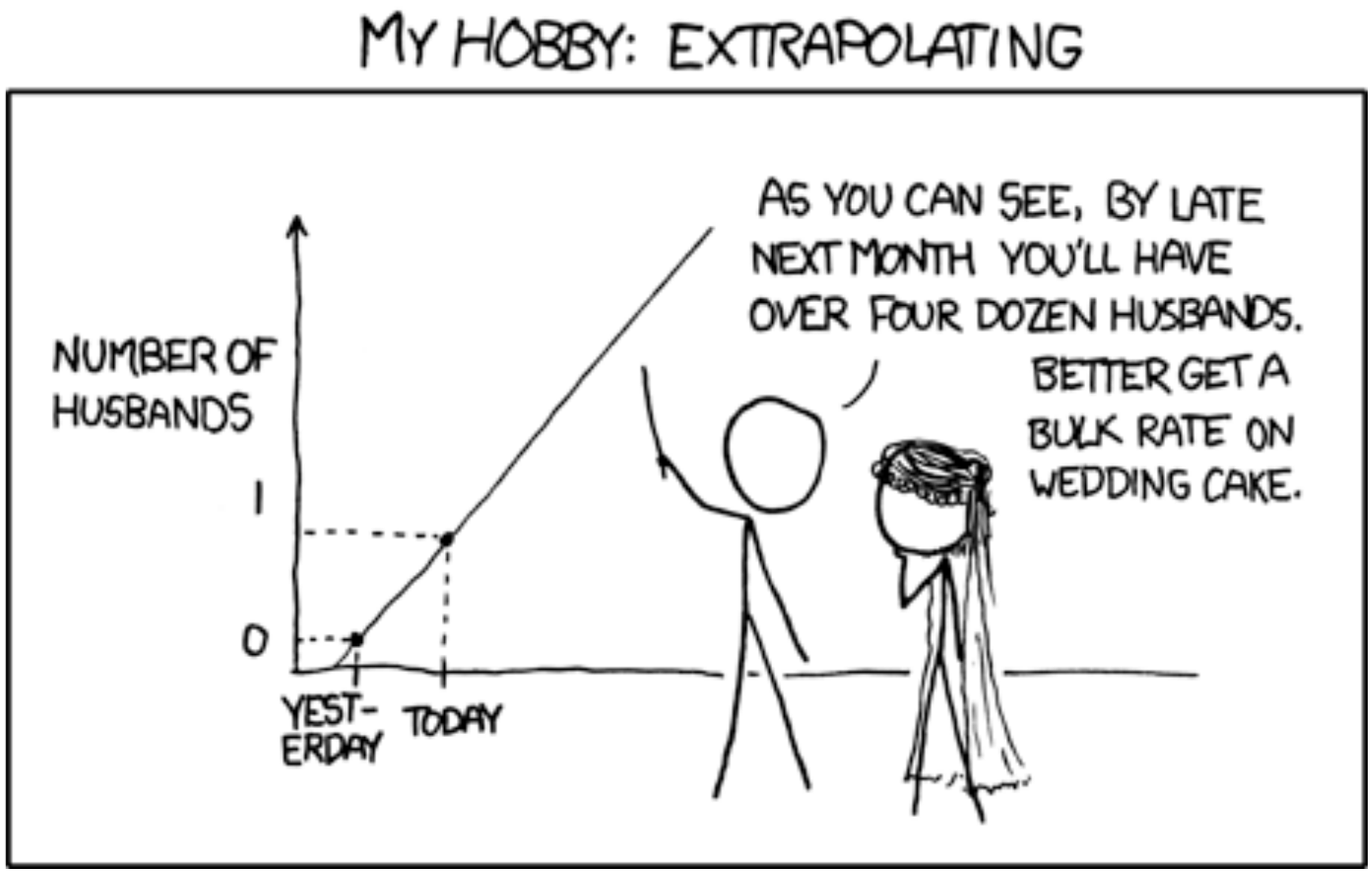


Gate t_{ox}



TID tolerance




MY HOBBY: EXTRAPOLATING
NUMBER OF HUSBANDS
1
0
YEST-ERDAY
TODAY
AS YOU CAN SEE, BY LATE NEXT MONTH YOU'LL HAVE OVER FOUR DOZEN HUSBANDS.
BETTER GET A BULK RATE ON WEDDING CAKE.

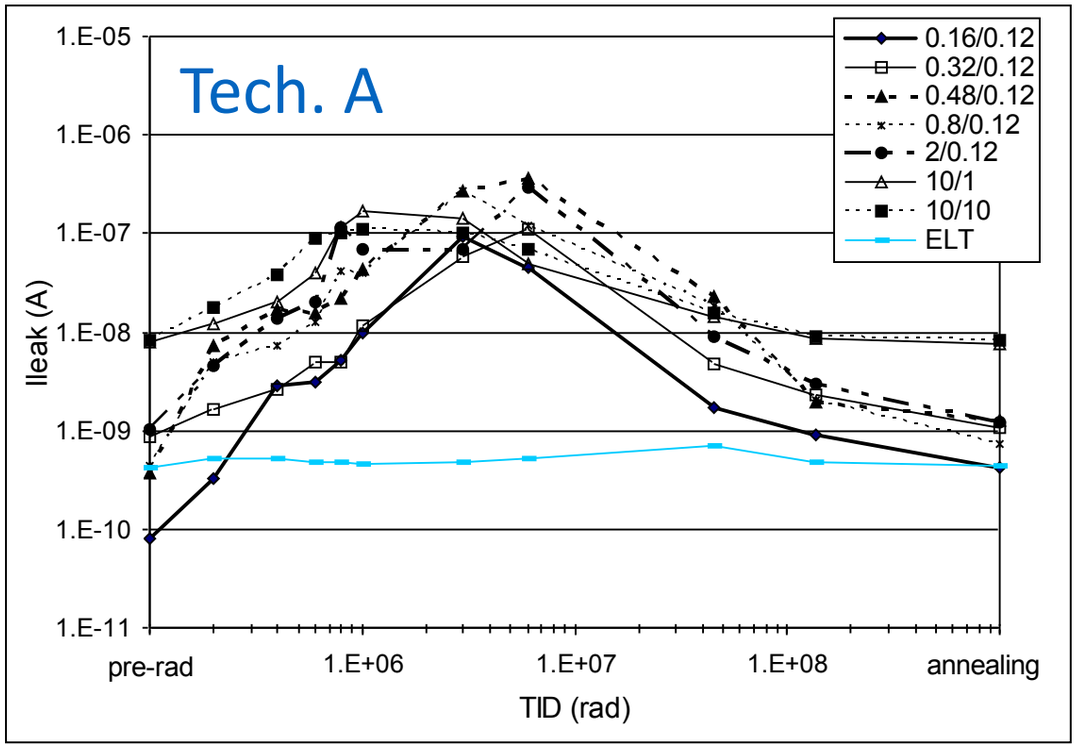
2003-2005: study of 130nm node in view of application in LHC upgrades

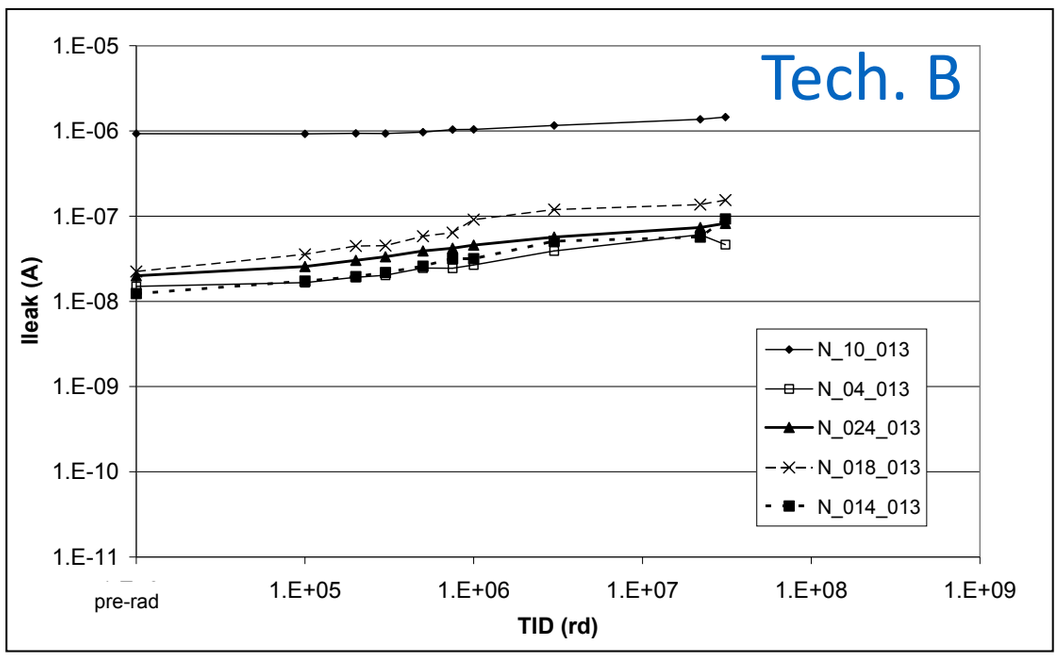
Samples from 3 different vendors were irradiated and measured

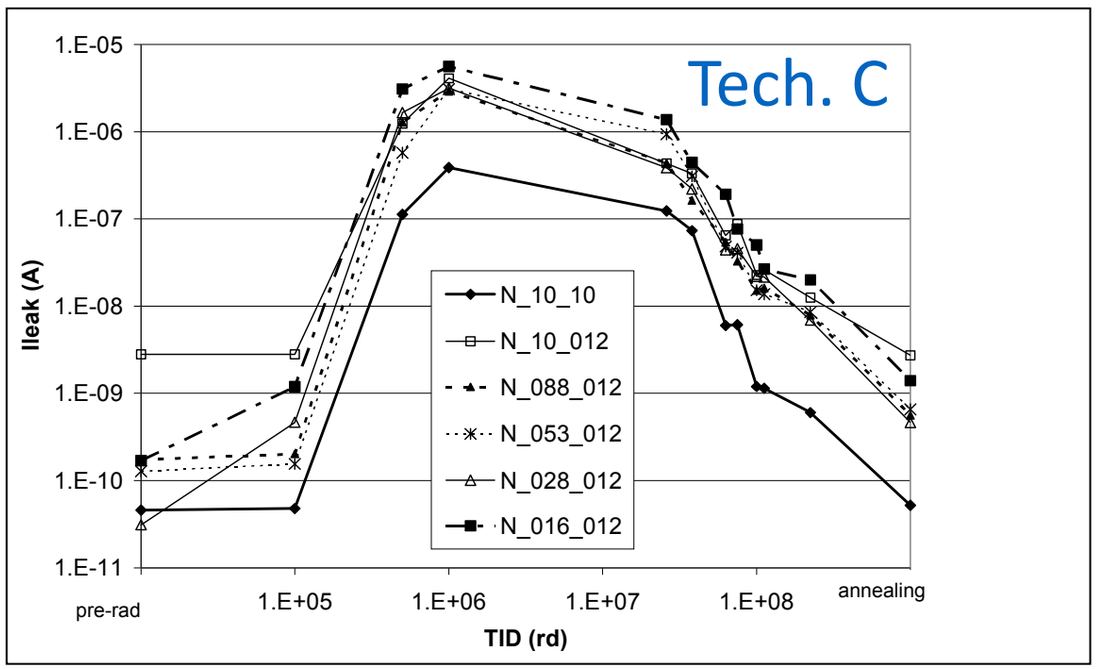
The gate oxide in the three 130nm technologies studied appeared to be compatible with applications in environments with multi-100Mrad TID levels

However, the leakage paths are technology dependent

(here shown for source-drain leakage currents in NMOS)

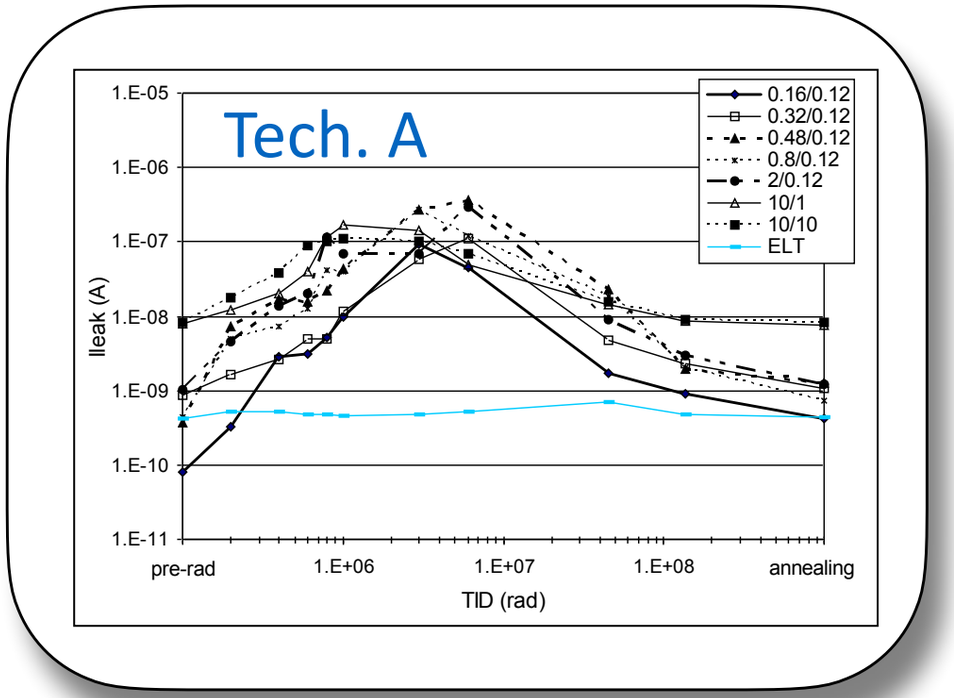






The selection of the manufacturer (Tech. A) was based on a number of criteria: long-term availability, cost, radiation tolerance, support offering, …

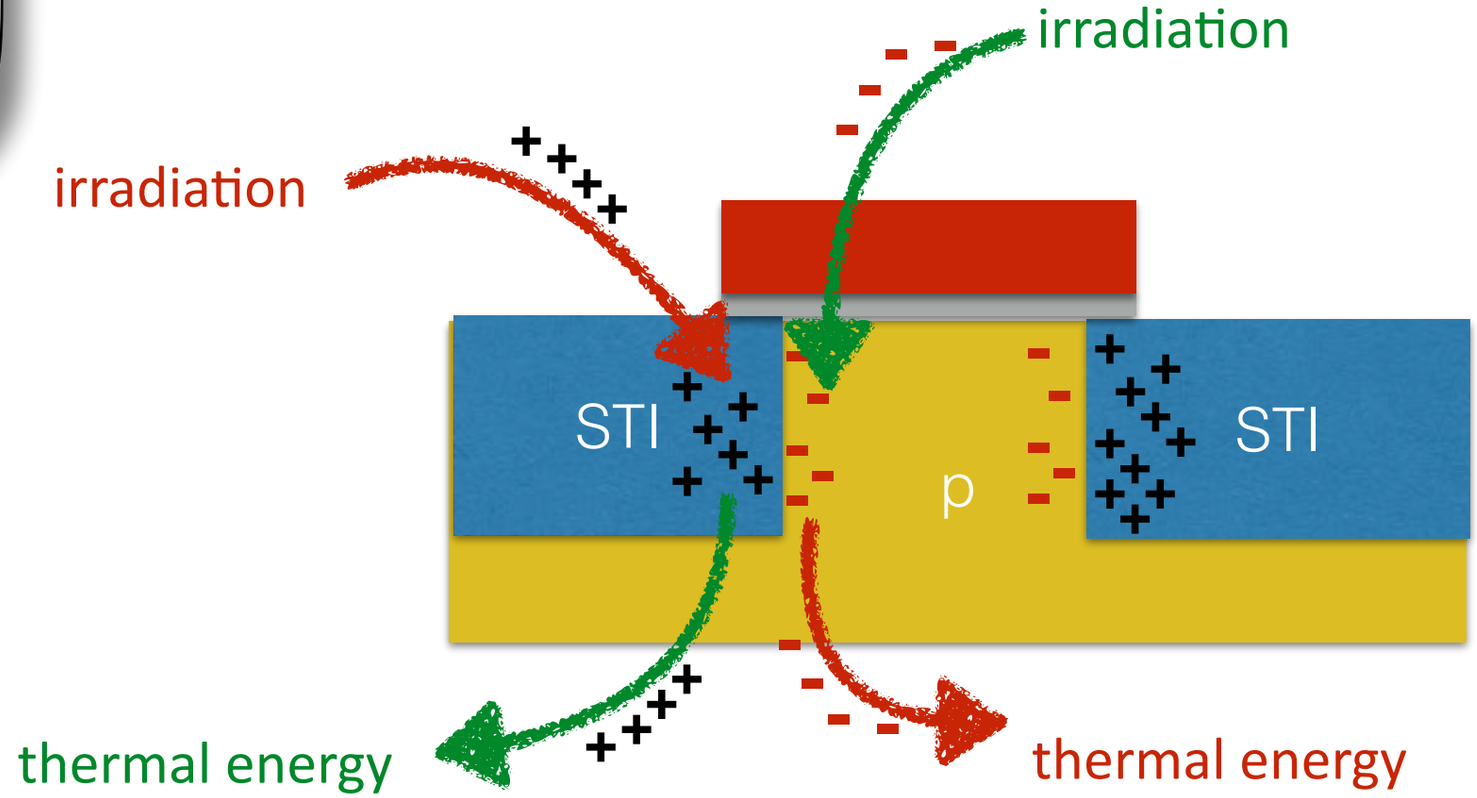
A large effort was dedicated to the characterisation of the selected technology



The leakage current is the sum of different mechanisms involving:

- the creation/trapping of charge (by radiation)
- its passivation/de-trapping (by thermal excitation)

These phenomena are Dose Rate and Temperature dependent!



Is there still the need for ELTs and guard rings?

No digital library with ELTs and guardrings was developed.
The standard cells library from a commercial supplier was considered usable

Designers have to evaluate if the leakage could threaten the circuit/system functionality in the application

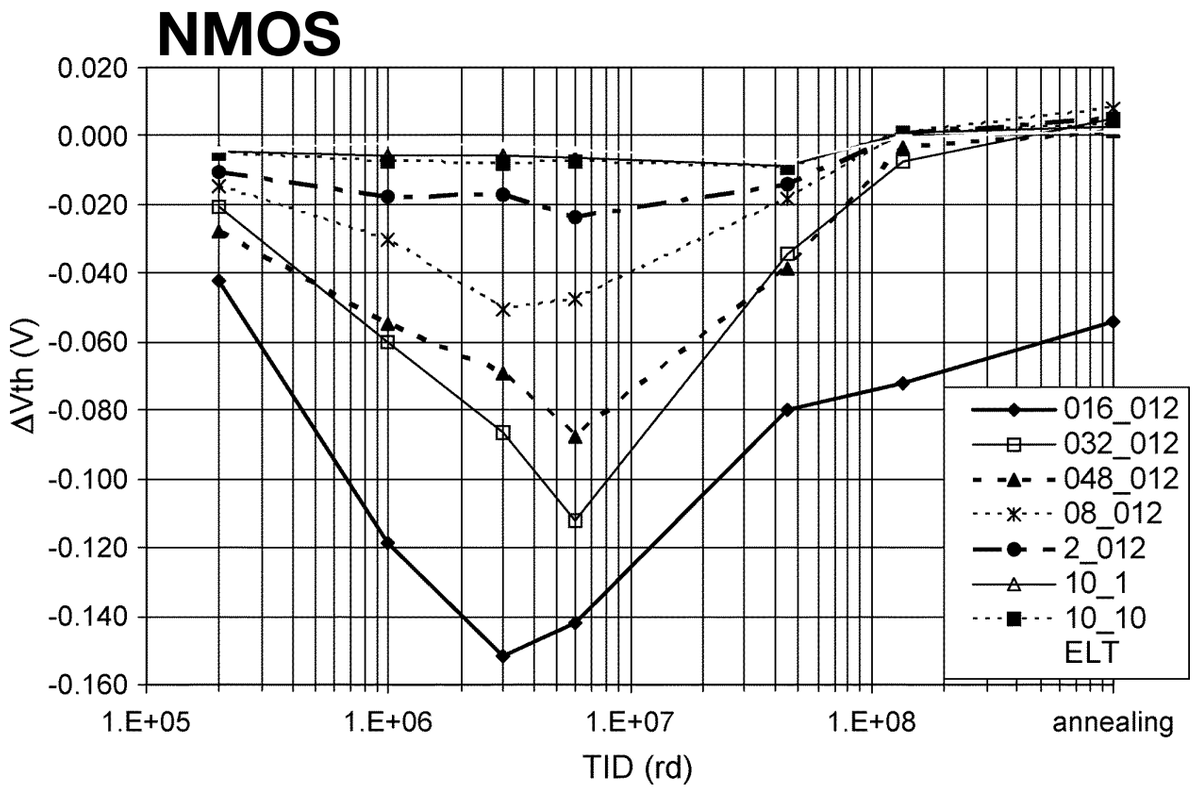
Flexibility & optimisation of performance

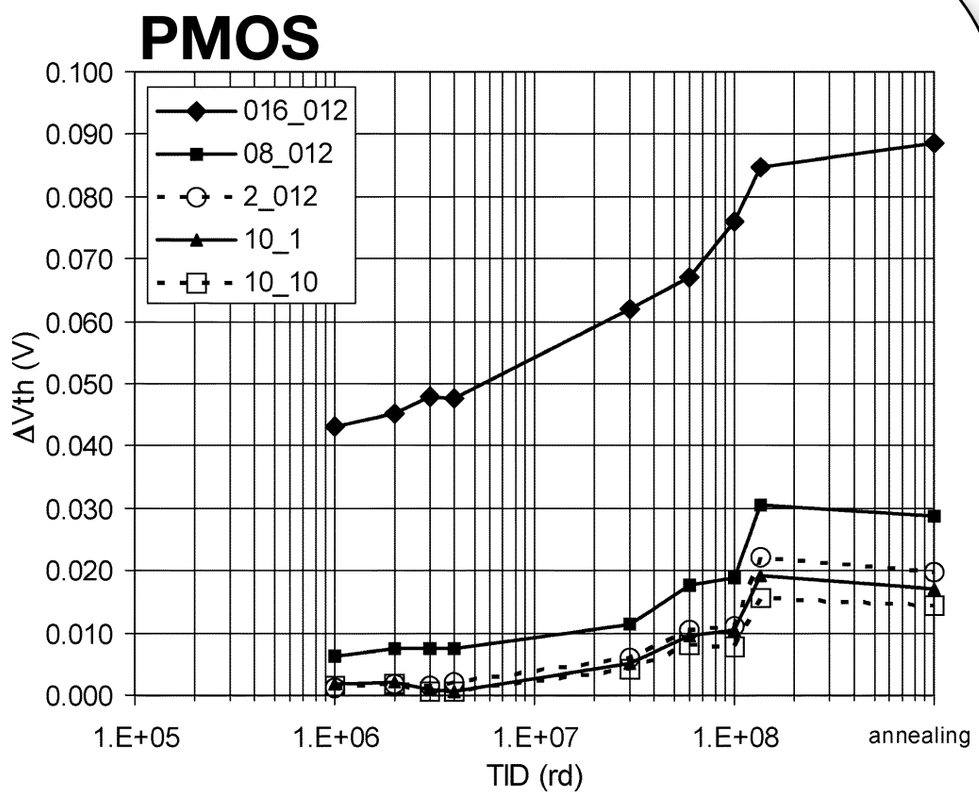
BUT

It requires system-specific risk assessment

RINCE (Radiation Induced Narrow Channel Effect): another radiation effect discovered in 130nm technology

This effect has then been observed in all studied technologies in the 350-28nm range



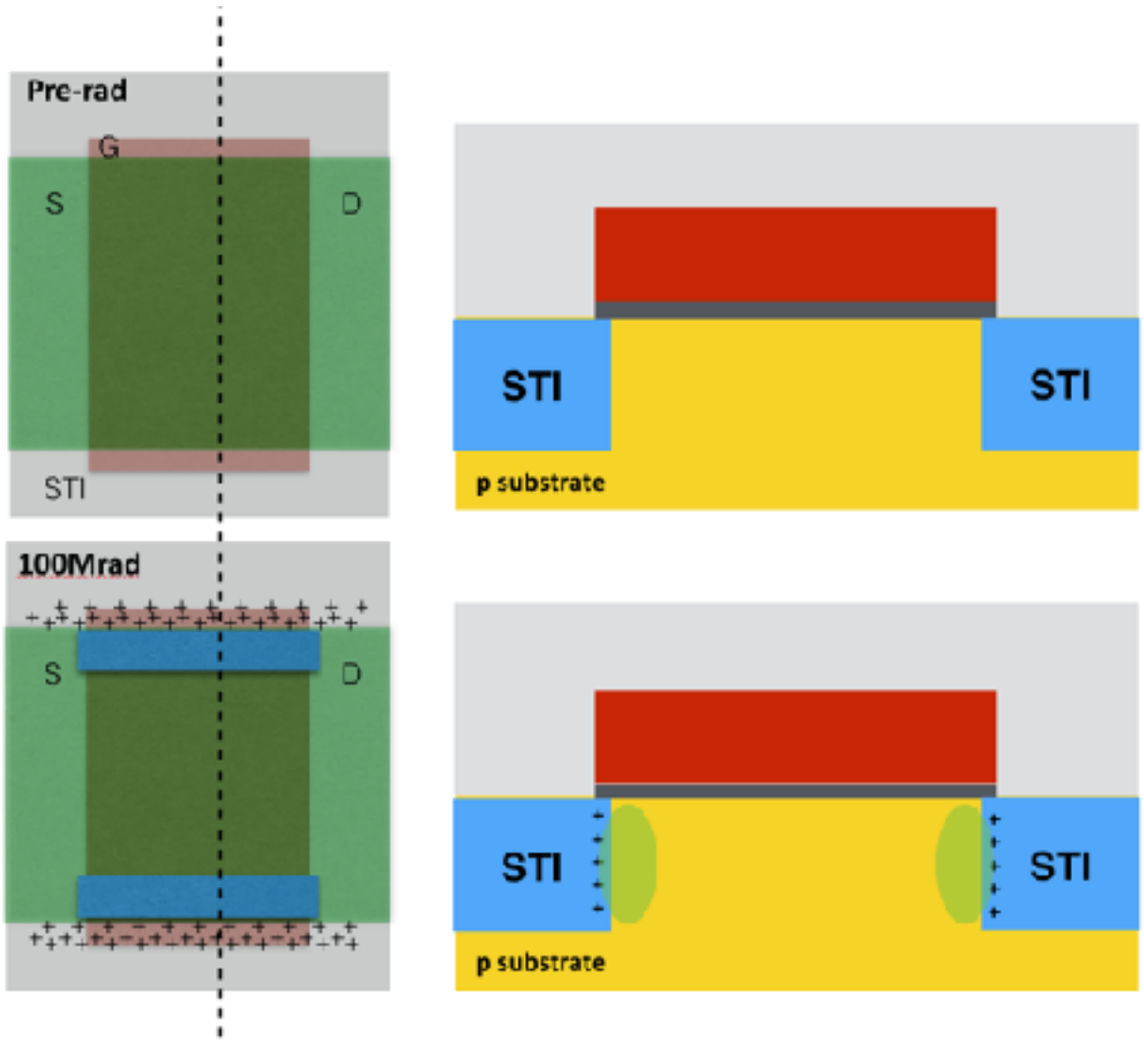


The degradation of the main transistor is W-dependent!

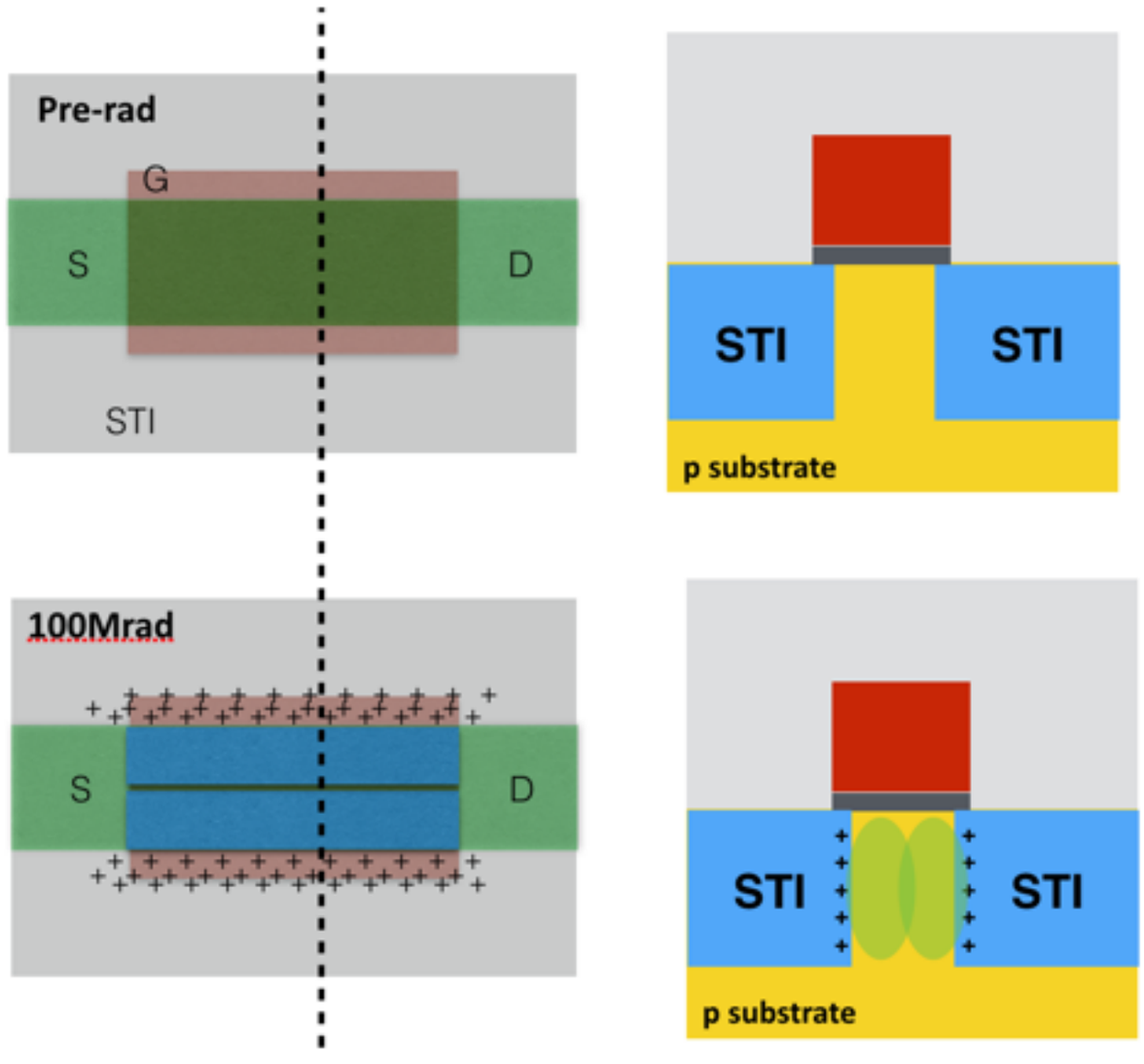
Conceptual representation of the RINCE

This effects is also traceable to charge trapping in a “parasitic” oxide (STI)

Wide channel transistor



Narrow channel transistor



Radiation hard processes

Hardness By Design (HBD) in commercial-grade processes

Production for LHC: 0.25um CMOS

Upgrades: 130nm CMOS

ca. 1998-2000

ca. 2006

time

TID up to 10Mrad

TID: 100Mrad

TID

Main transistor

V_{th}, g_m, …

Leakage in parasitics

Leakage in parasitics

Leakage in parasitics

RINCE

Outline

Introduction to ASICs and CMOS technologies

Fundamentals of radiation effects

Radiation effects in CMOS technologies

A brief history of radiation-tolerant ASIC development for LHC

The first generation of LHC experiments: 0.25µm CMOS

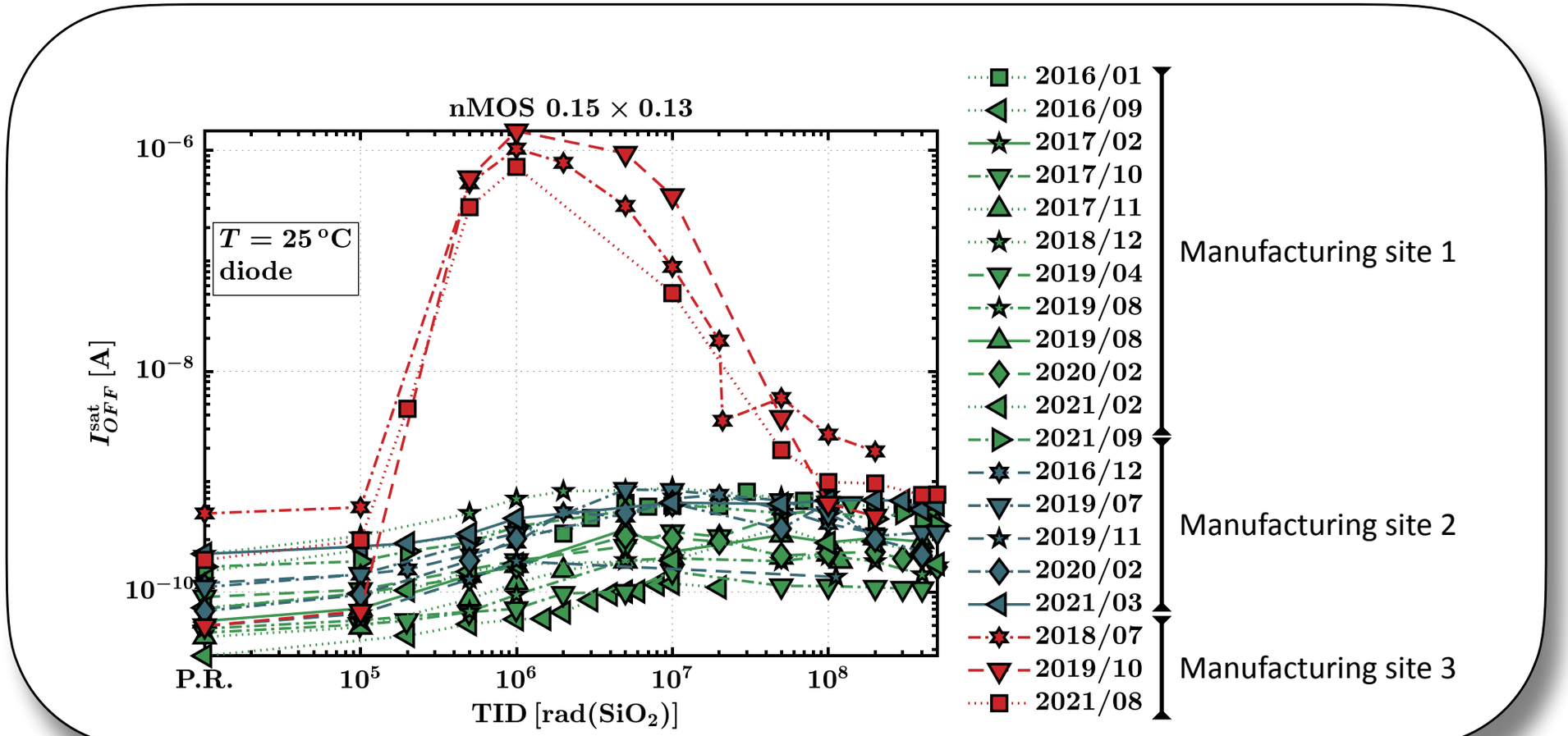
130nm CMOS for the upgrades

Higher radiation levels for HL-LHC: new effects

Case Studies

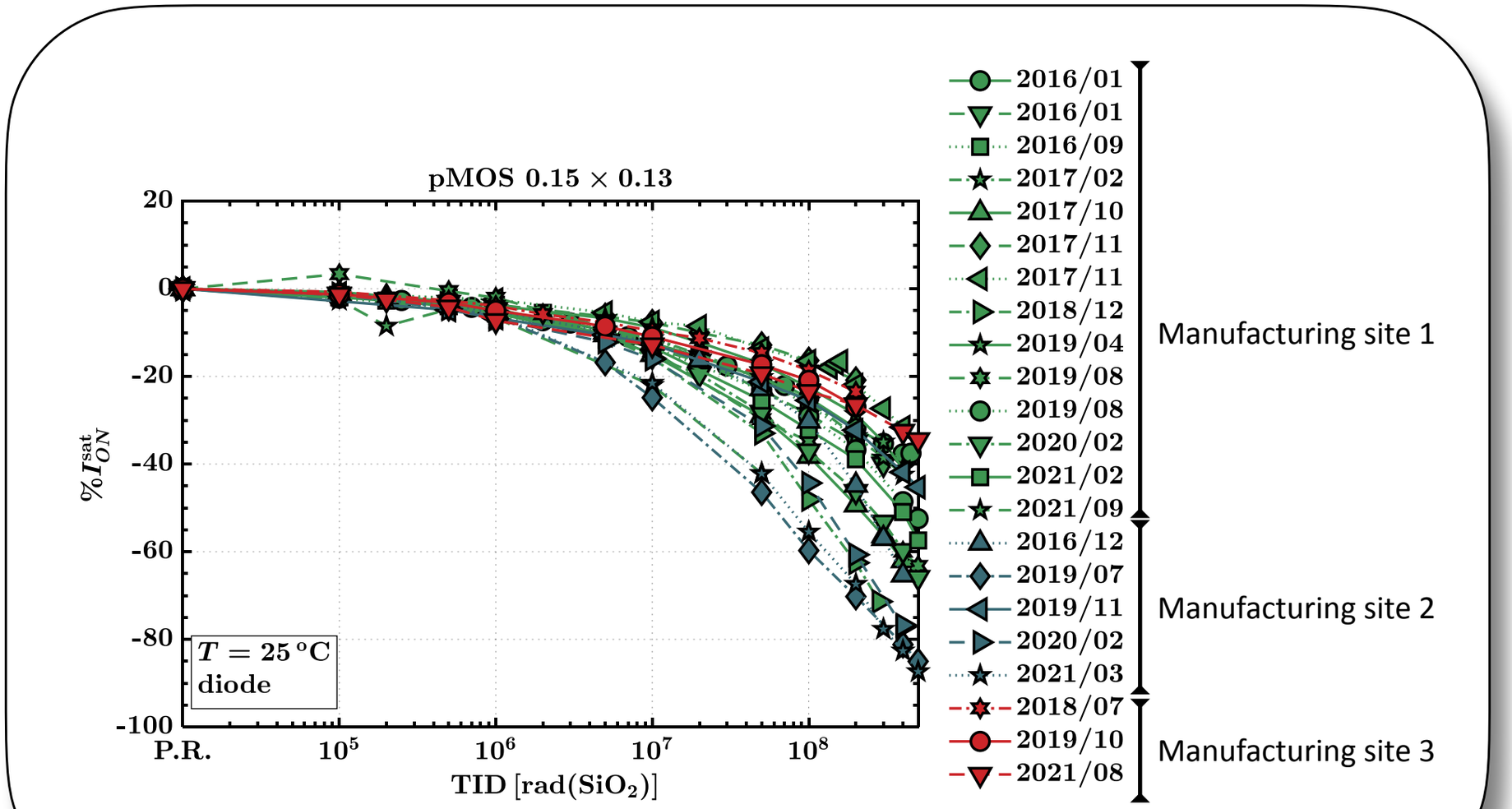
Concerns about long-term availability of the 130nm from “Supplier A” drove the selection of a backup supplier, that gradually has become the main supplier since.

The leakage current evolution in NMOS transistors strongly varies between hardware fabricated in different manufacturing sites (Fabs).



- Require production in Manufacturing sites 1 and 2 (is it possible?)
- Verify the radiation response of every production run!

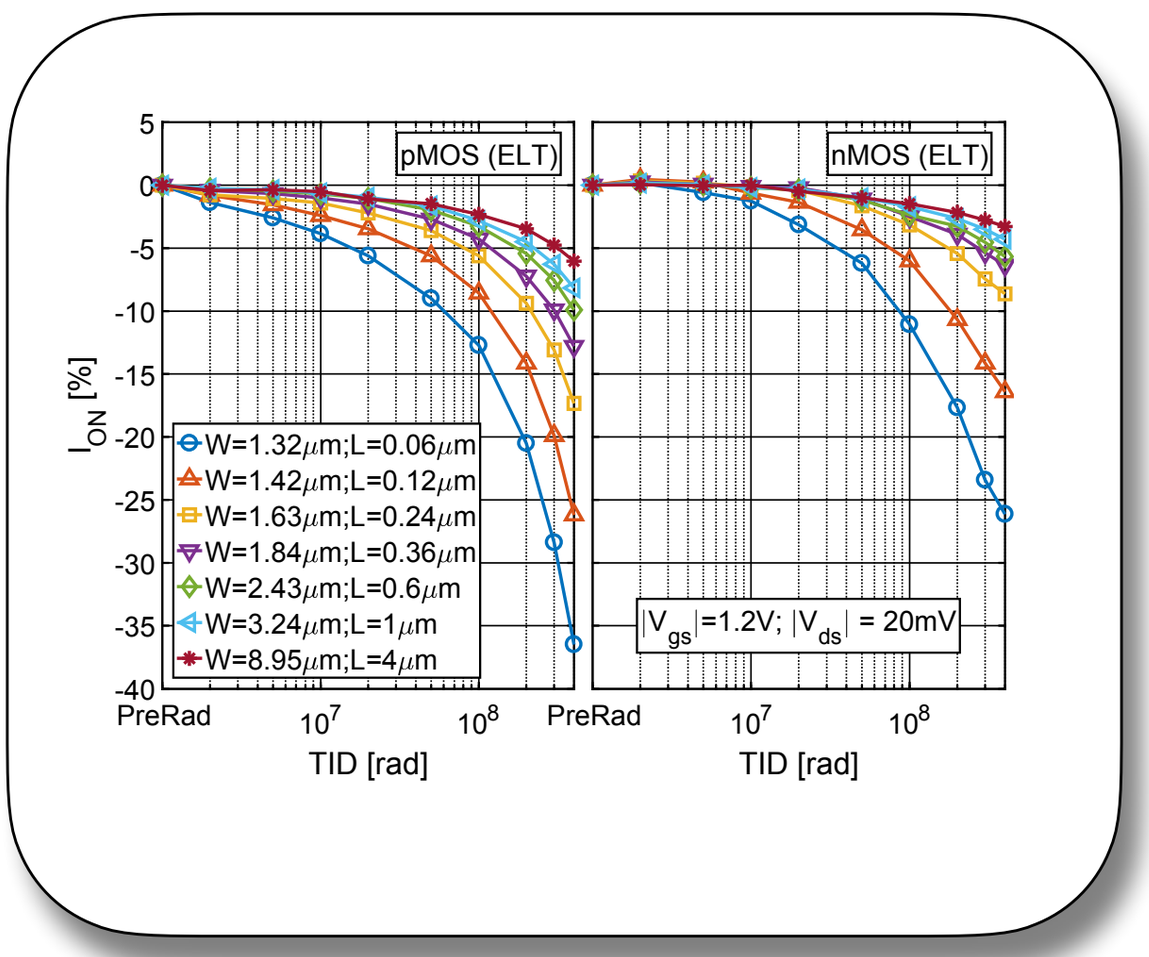
The radiation response of test transistors included in every manufacturing run highlights a relevant lot-to-lot variability at high TID, for PMOS transistors.

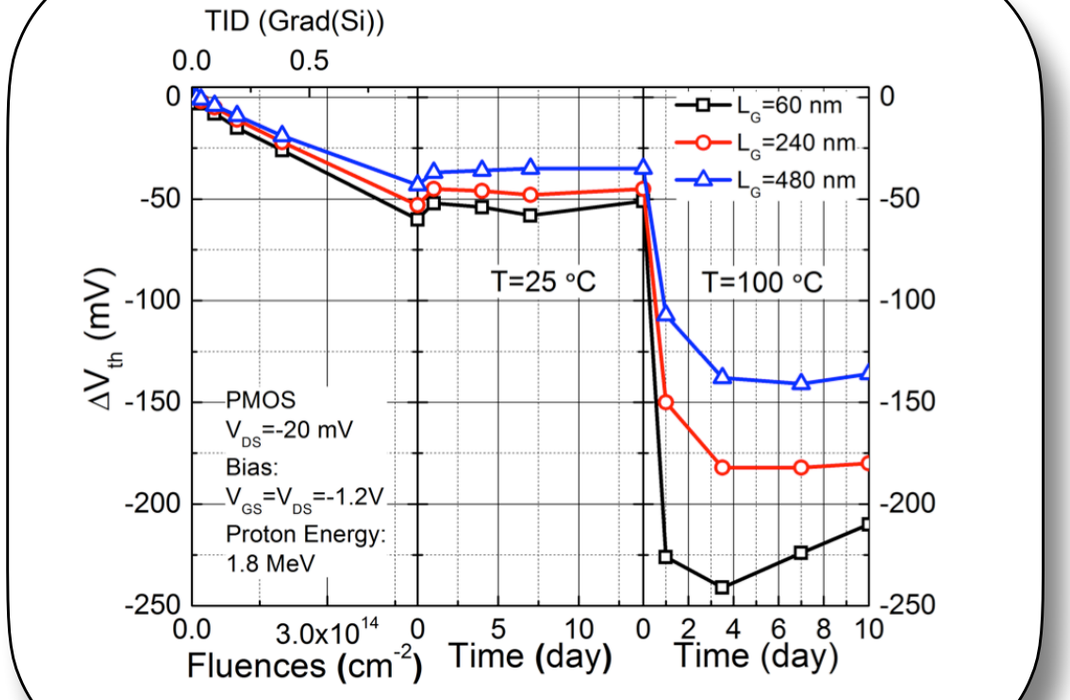


- Take design margins to account for this variability in degradation
- Verify the radiation response of every production run!

For some HL-LHC detectors, the adoption of the 65nm technology was required.

The study of TID effects in transistors revealed the presence of new mechanisms at very high TID levels.

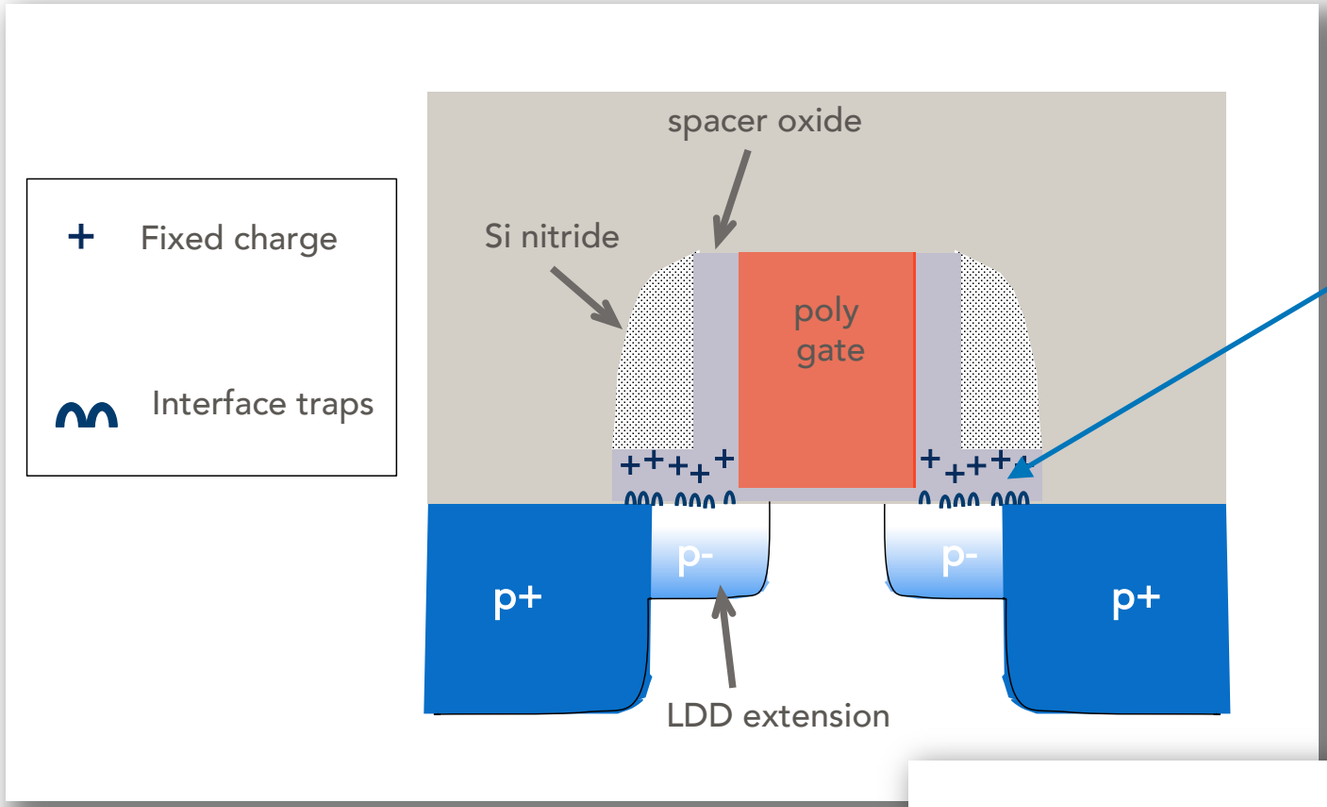




Radiation Induced Short Channel Effect (RISCE)

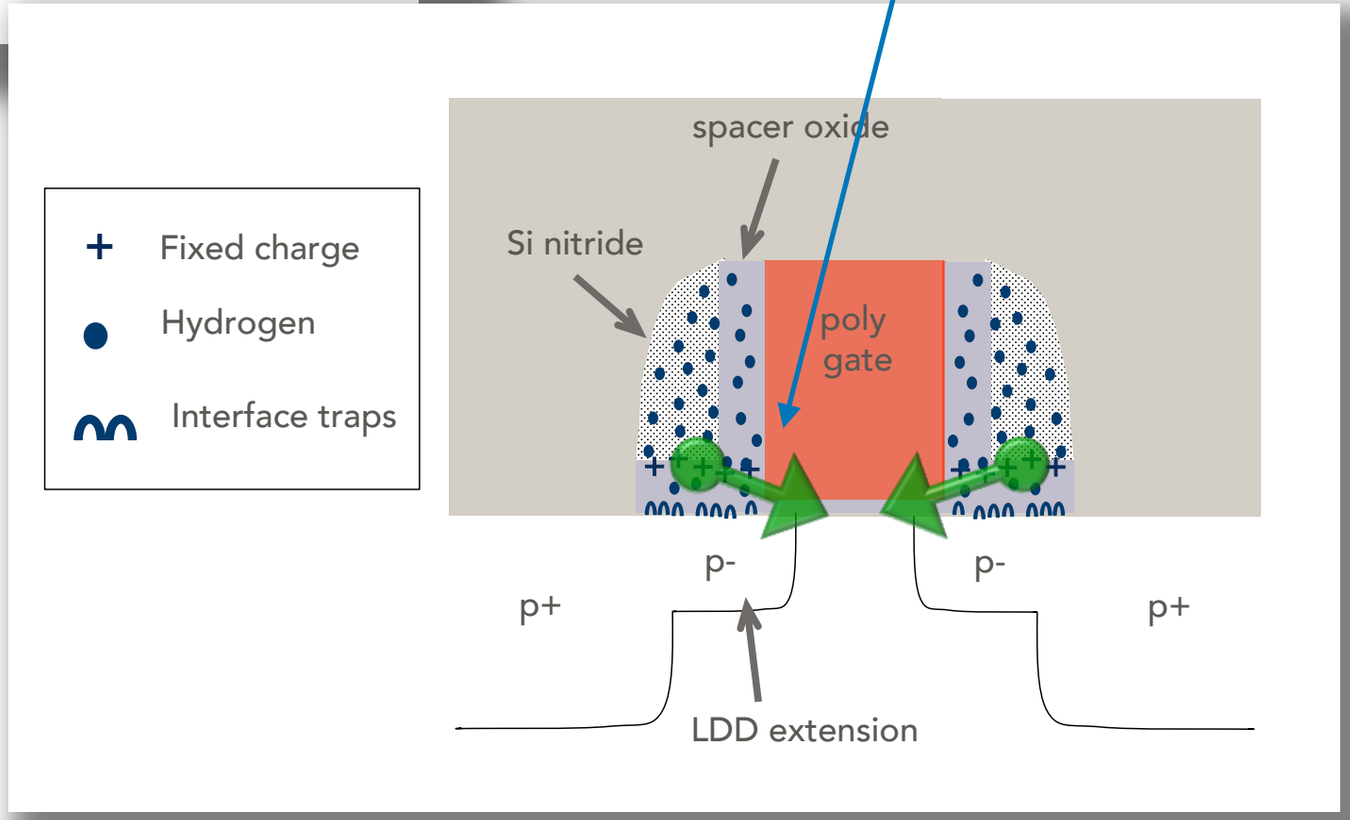
The complex mechanisms behind the RISCE is understood

Origin: radiation effects in the spacer oxide (another “parasitic” structure)



Defects in the space oxide: change in effective doping in the LDD extensions = increase in series resistance

Hydrogen migration from spacers introduces defects in the thin gate oxide



after F.Faccio et al., “Influence of LDD spacers and H+ transport on the total-ionizing-dose response of 65 nm MOSFETs irradiated to ultra-high doses”, IEEE TNS Vol.65, N.1, Jan.2018

Radiation hard processes

Hardness By Design (HBD) in commercial-grade processes

Production for LHC: 0.25um CMOS

Upgrades: 130nm CMOS

(some) tracker upgrades: 65nm CMOS

ca. 1998-2000

ca. 2006

ca. 2014

time

TID up to 10Mrad

TID: 100Mrad

TID: 400Mrad

TID: 100Mrad to 1Grad

TID

Main transistor

V_{th}, g_m, …

Leakage in parasitics

Leakage in parasitics

Leakage in parasitics

RINCE

Leakage in parasitics

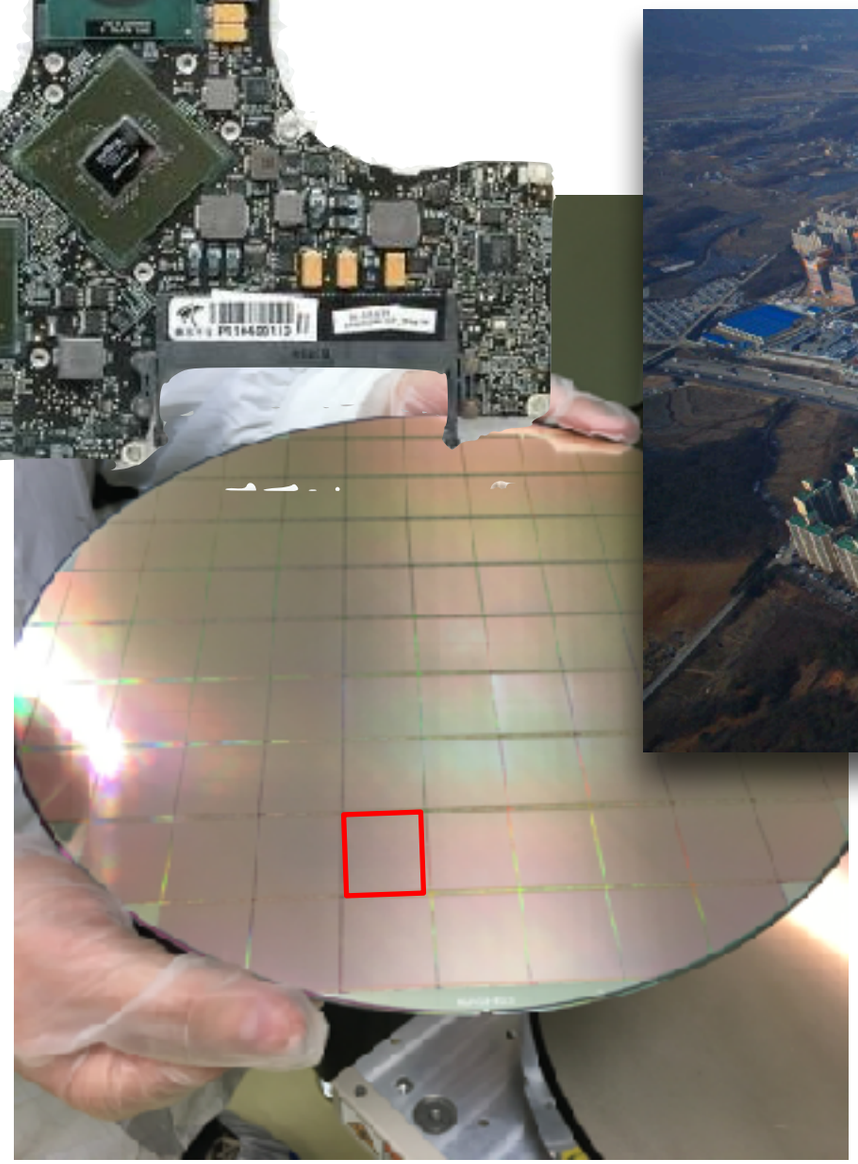
RINCE

RISCE

Summary

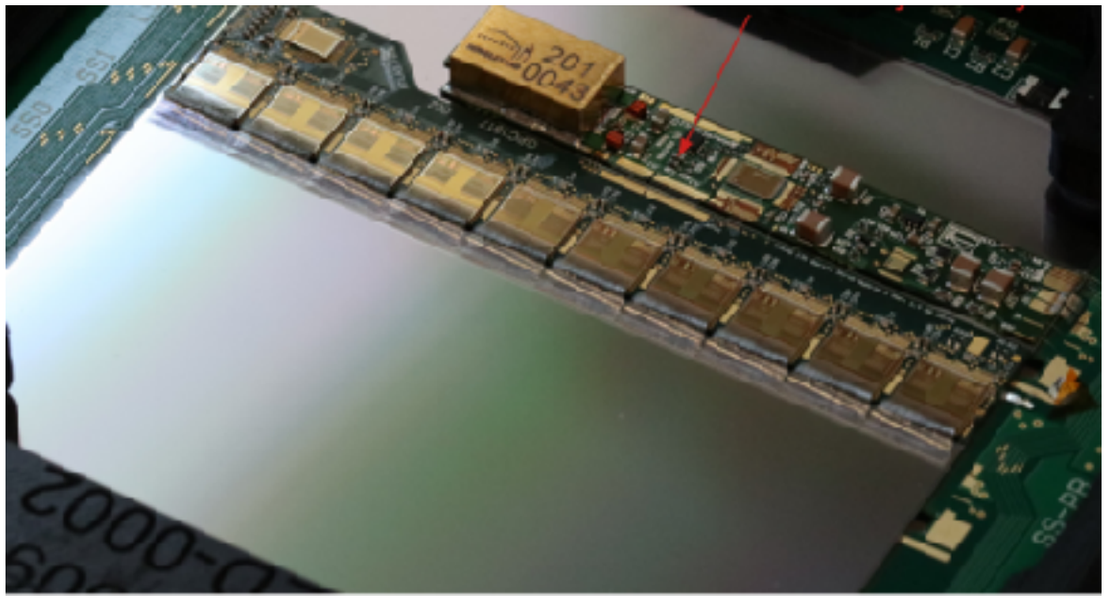
Summary

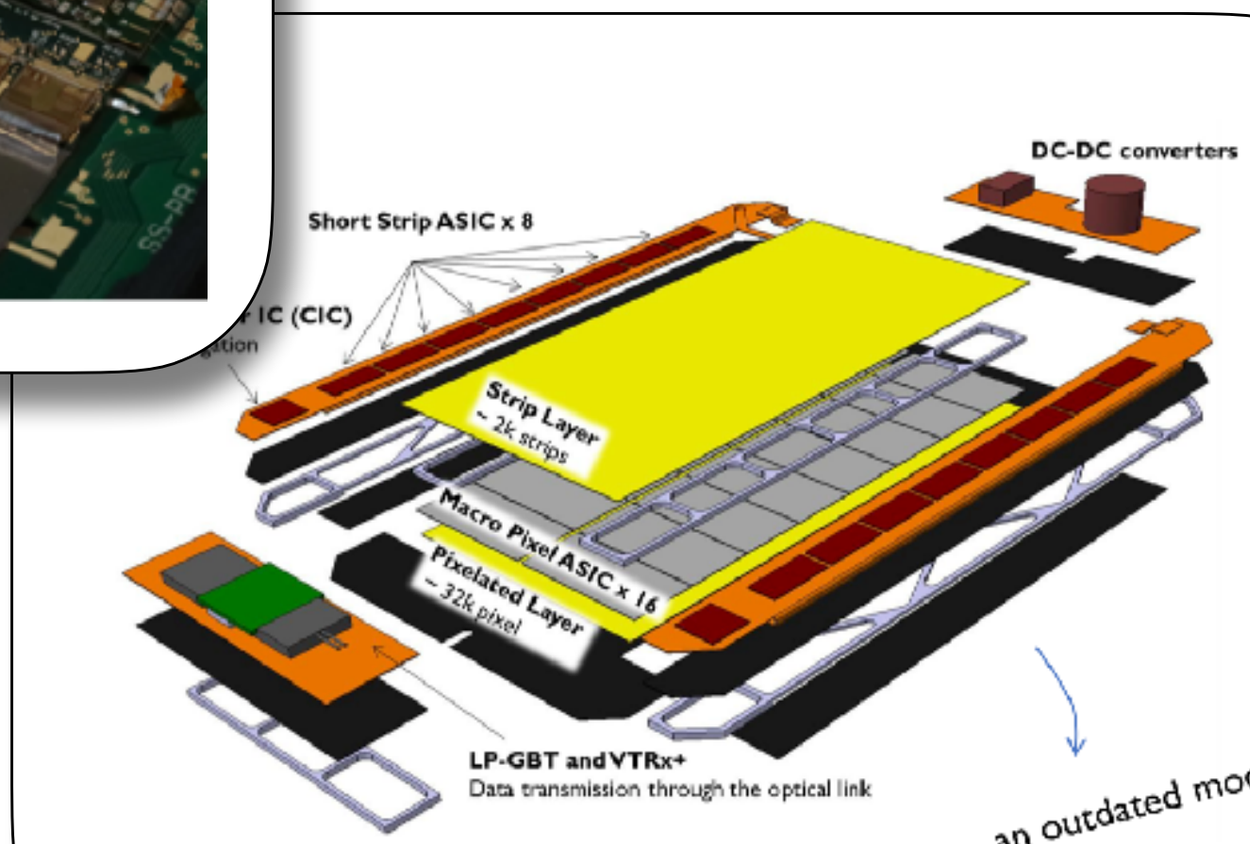
Integrated Circuits are everywhere and their manufacturing requires massive investments



Summary

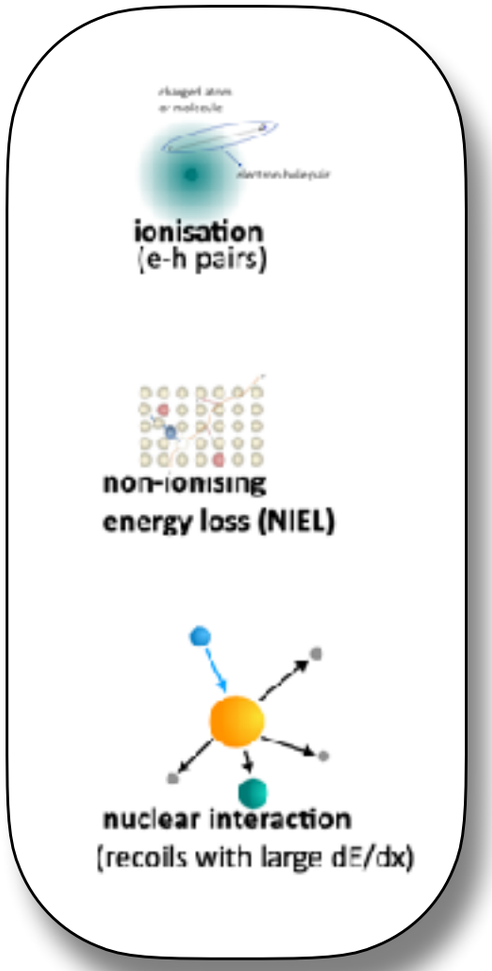
The physics performance of LHC experiments largely relies on ASICs

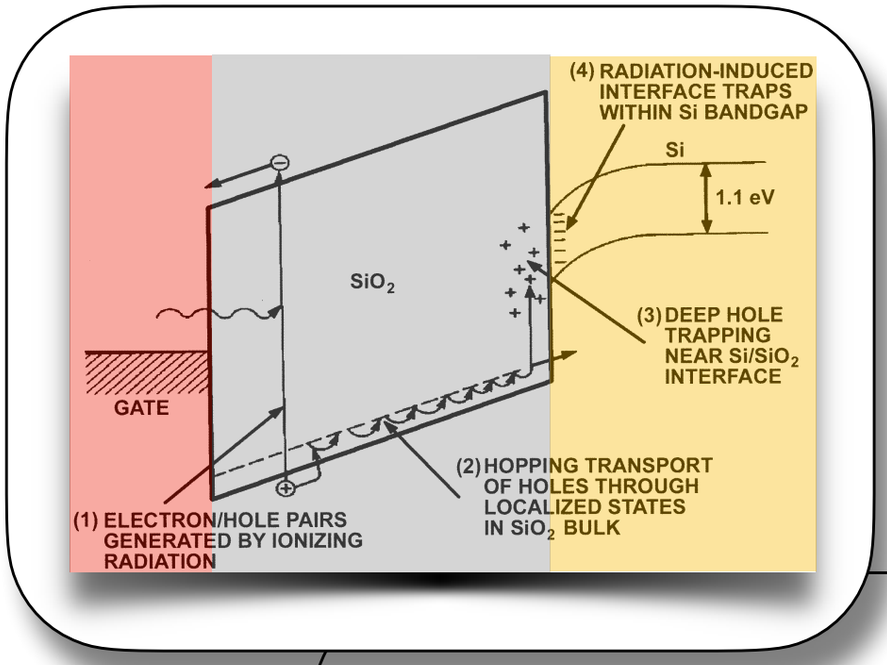


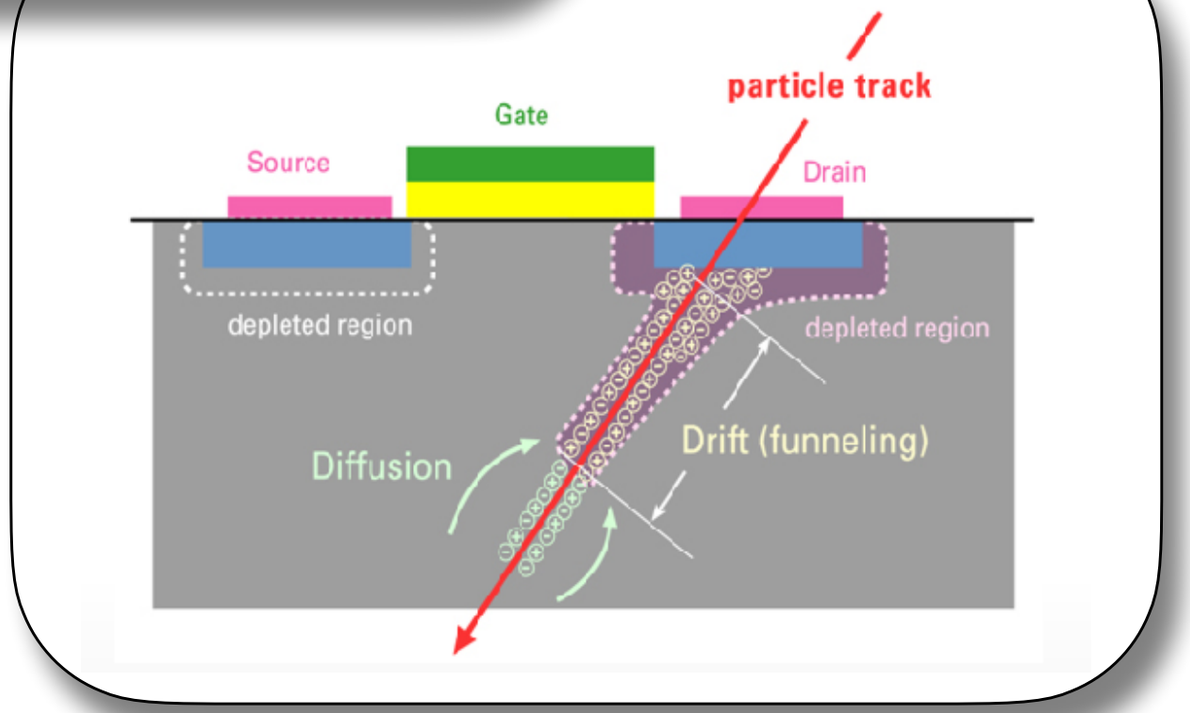


Summary

The reliable functionality of ASICs is threatened by radiation: TID, (displacement damage)**, SEE**

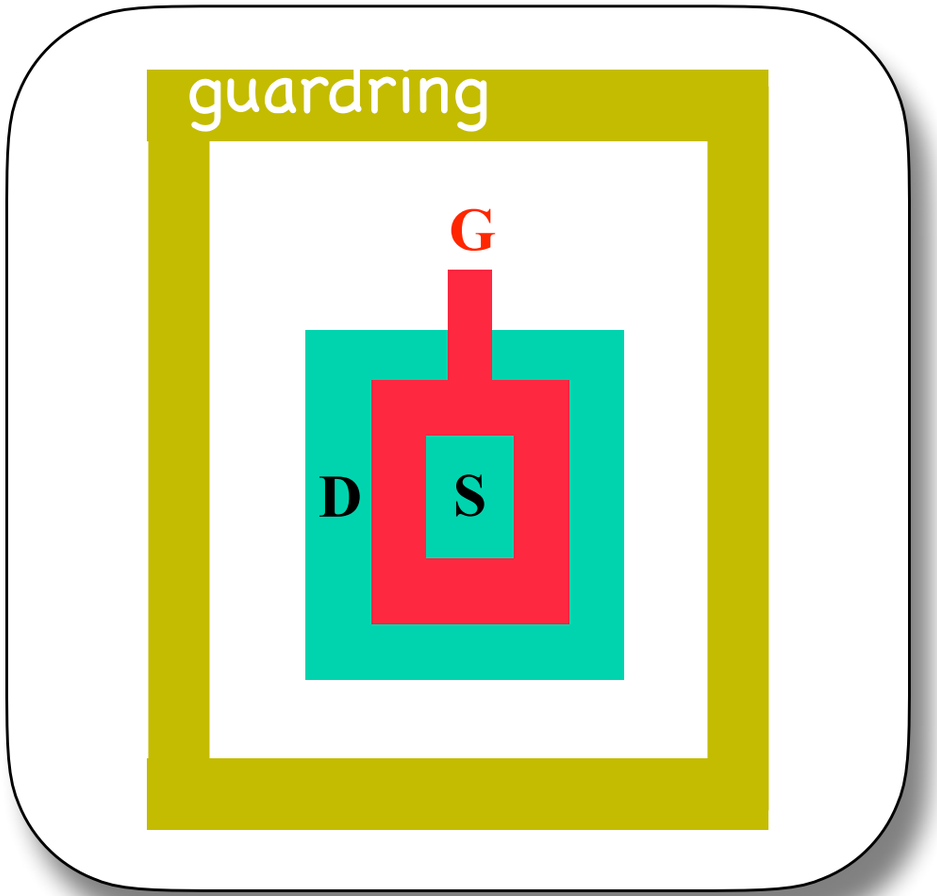


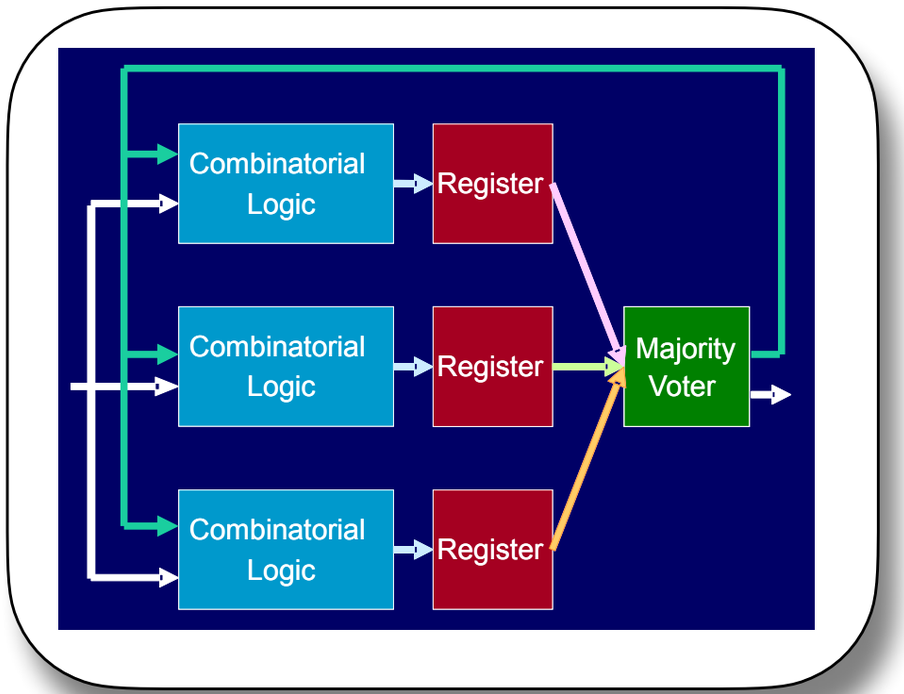




Summary

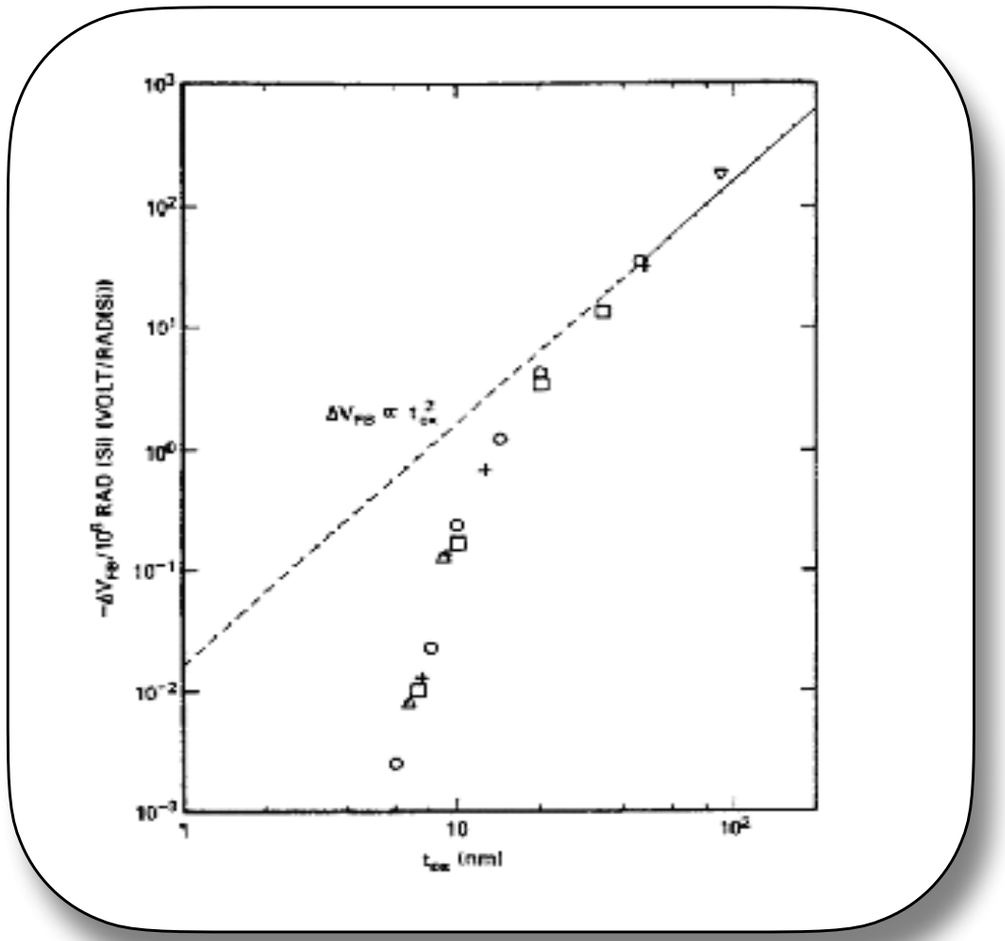
ASICs can be made tolerant to radiation using dedicated design techniques: Hardness By Design
(transistor shape like ELT, guard-rings, substrate contacts, transistor size, triplication, encoding, …)





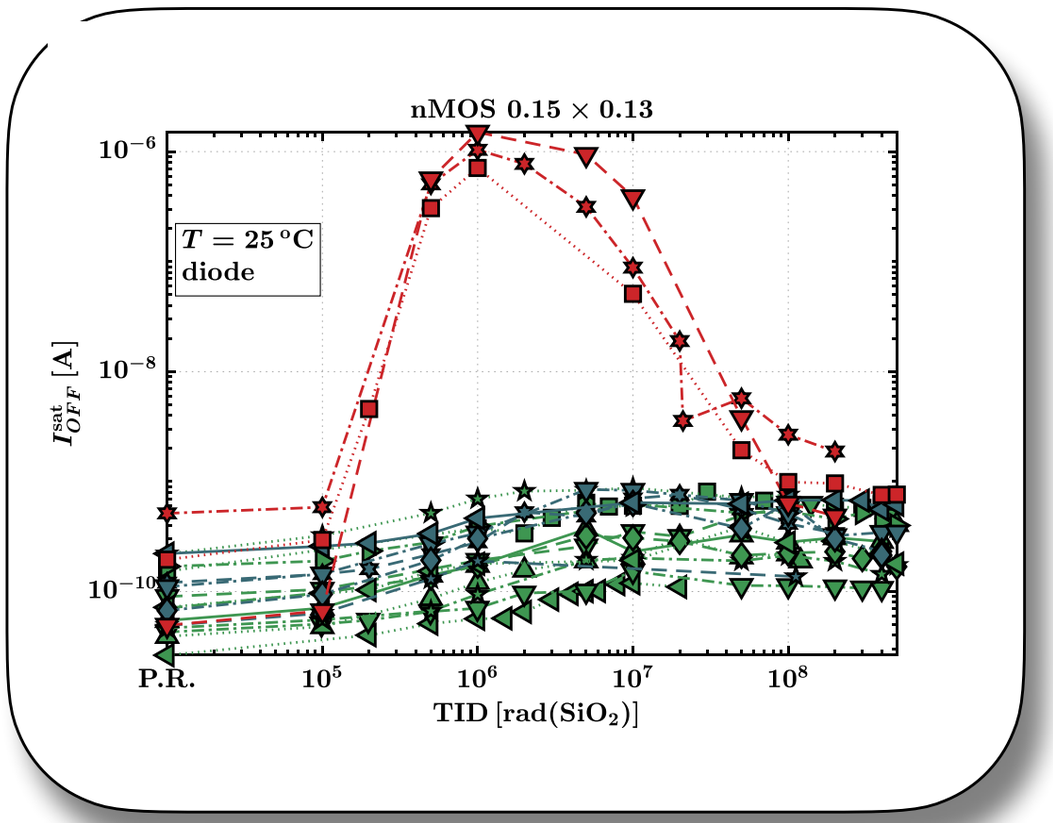
Summary

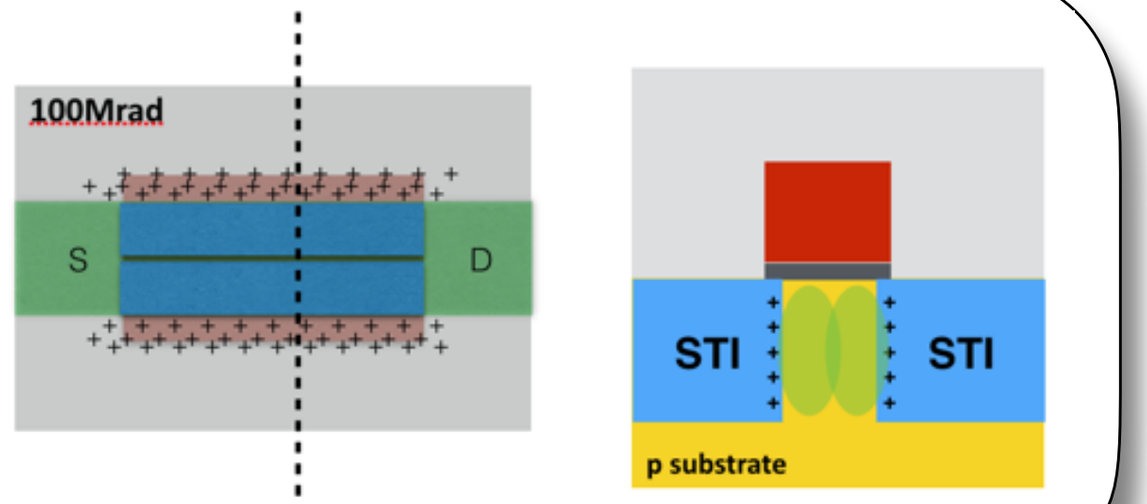
The thin gate oxide of scaled down CMOS technologies is less sensitive to TID effects.

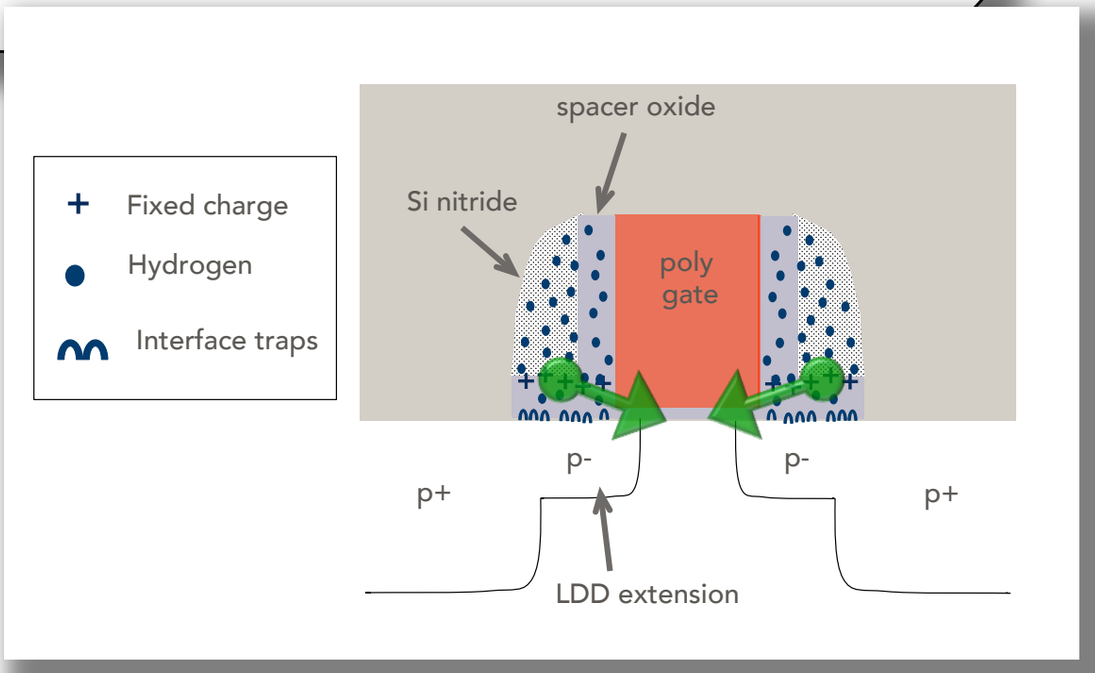


Summary

Parasitic oxides (STI, spacer) dominate the TID response and they particularly affect narrow and short transistors (RINCE, RISCE). This determines a potentially large variability in the radiation response (Fab-to-Fab, lot-to-lot)







Summary

Integrated Circuits are everywhere and their manufacturing requires massive investments

The physics performance of LHC experiments largely relies on ASICs

The reliable functionality of ASICs is threatened by radiation: TID, (displacement damage), SEE

ASICs can be made tolerant to radiation using dedicated design techniques: Hardness By Design
(transistor shape like ELT, guard-rings, substrate contacts, transistor size, triplication, encoding, …)

The thin gate oxide of scaled down CMOS technologies is less sensitive to TID effects.

Parasitic oxides (STI, spacer) dominate the TID response and they particularly affect narrow and short transistors (RINCE, RISCE). This determines a potentially large variability in the radiation response (Fab-to-Fab, lot-to-lot)

The radiation levels for HL-LHC electronics are MUCH LARGER than anywhere else.
Reliable functionality in this environment is VERY CHALLENGING.
Using scaled-down CMOS technologies for ASICs helps, but does not make the job easy.

Outline

Introduction to ASICs and CMOS technologies

Fundamentals of radiation effects

Radiation effects in CMOS technologies

A brief history of radiation-tolerant ASIC development for LHC

The first generation of LHC experiments: 0.25µm CMOS

130nm CMOS for the upgrades

Higher radiation levels for HL-LHC: new effects

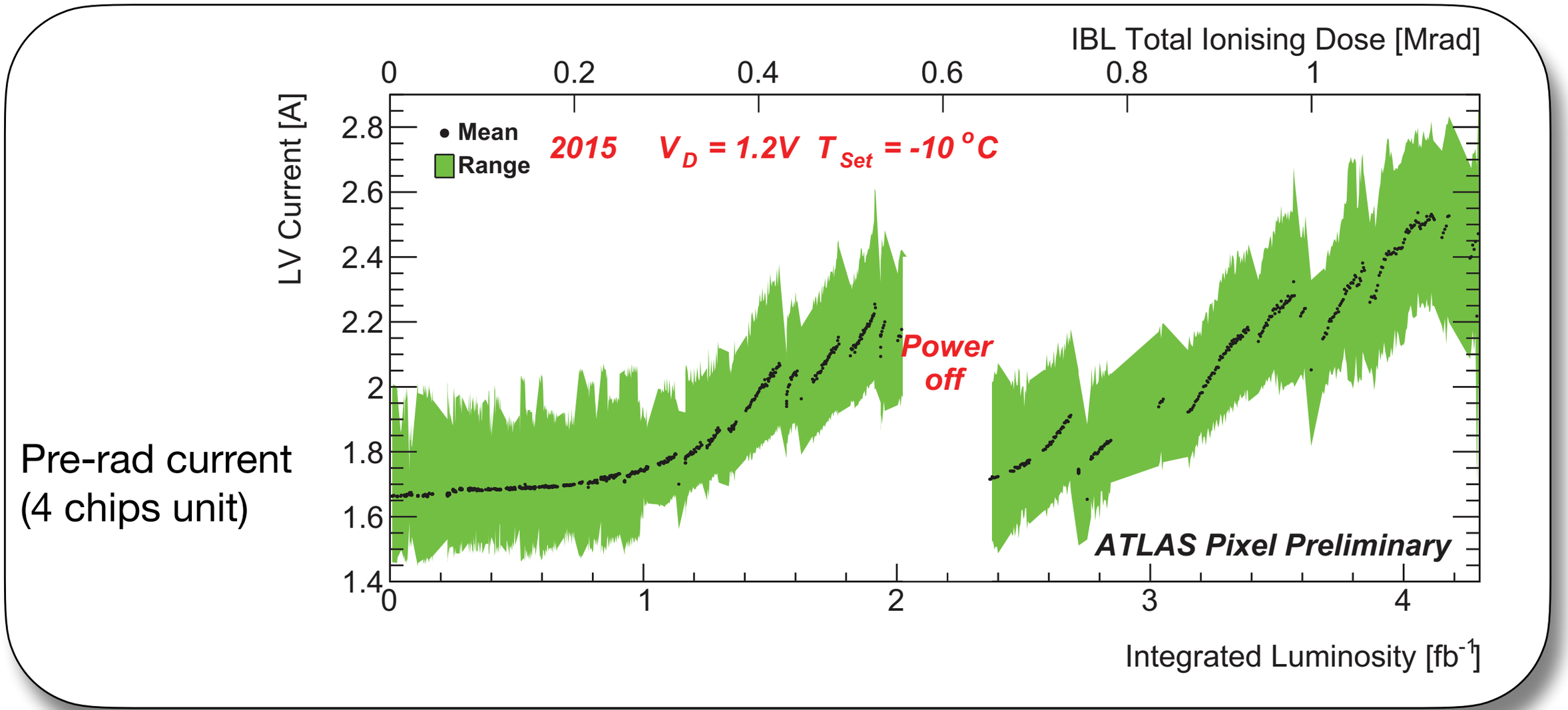
Case Studies

Case study 1

The increase in power consumption in 130nm ASICs

FE-I4 is the readout ASIC for the ATLAS pixel insertable b-layer (IBL) added to the experiment in 2014 and operational since 2015.

Early in its operational life, it showed an increase in the current consumption requiring a power off…

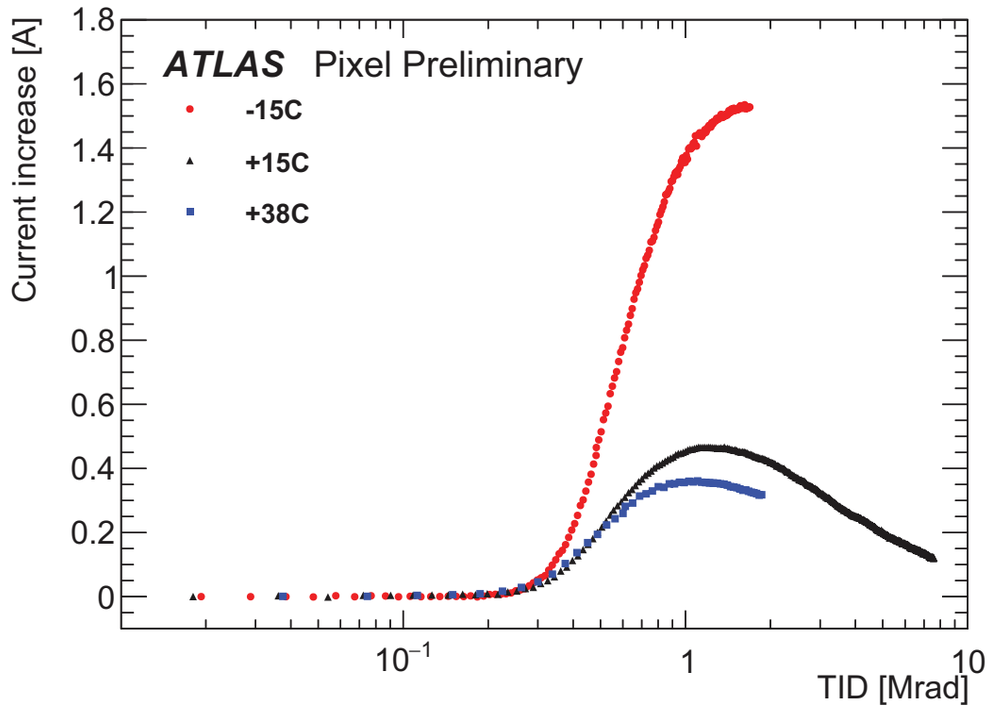


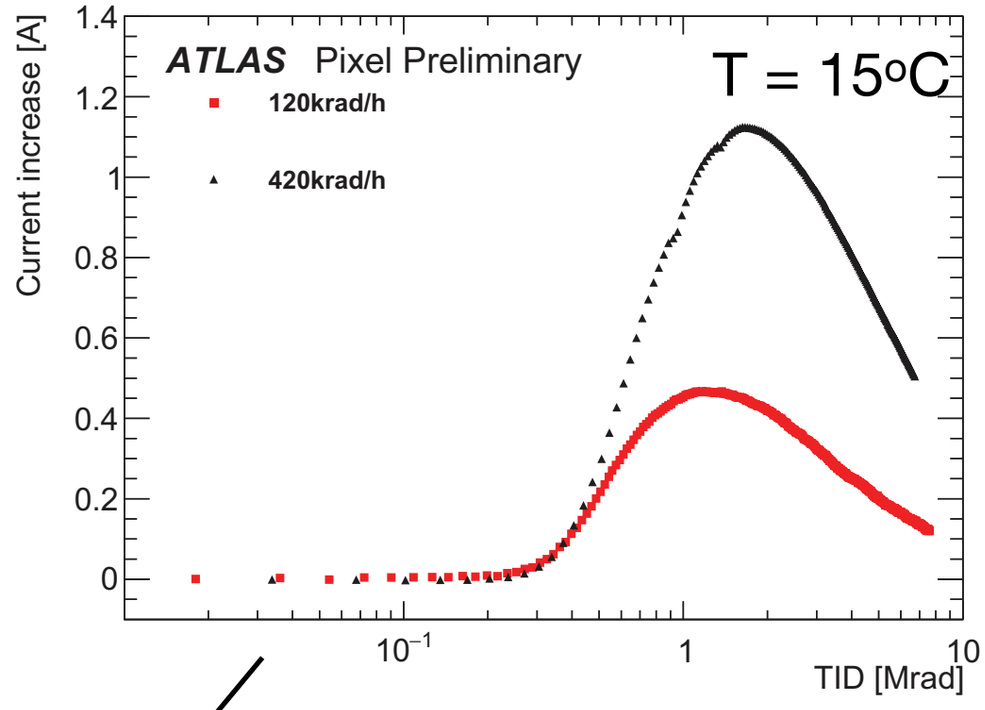
Pre-rad current
(4 chips unit)

Images from: A.La Rosa, "Irradiation induced effects in the FE-I4 front-end chip of the ATLAS IBL detector", IEEE NSS 2016

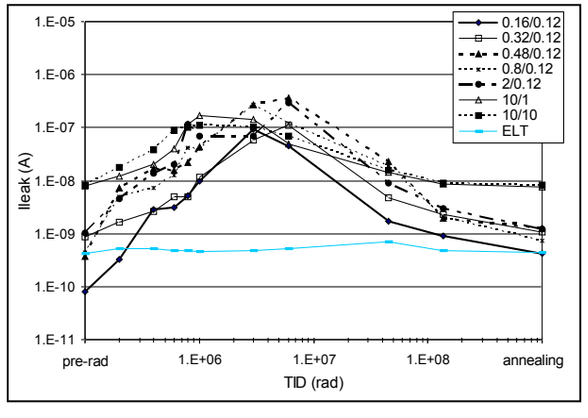
The increase of the power consumption is due to radiation-induced leakage current in the FE-I4 ASIC, strongly dependent on temperature and dose rate

Pre-rad current = 380mA



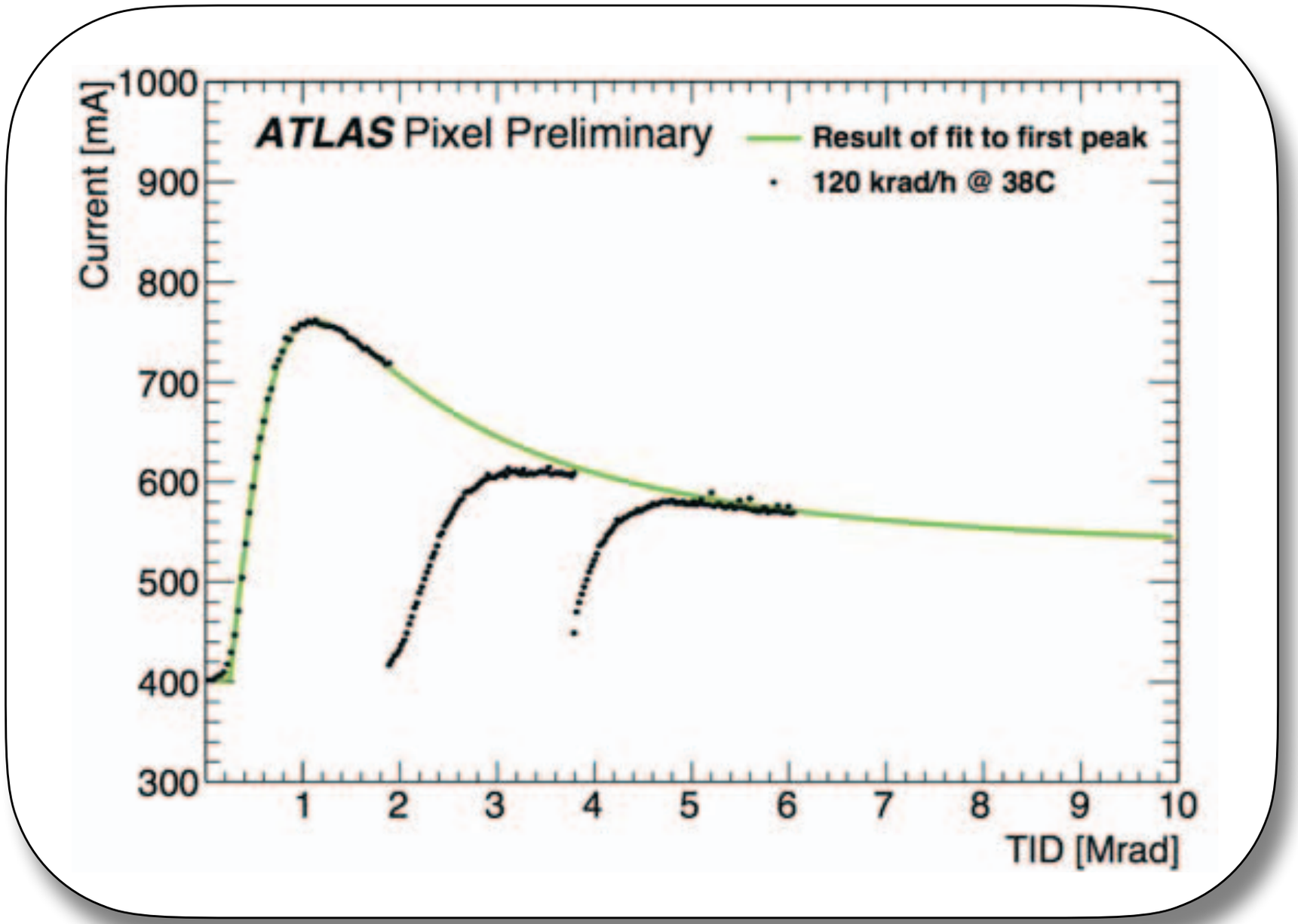


Similar to source-drain leakage in NMOS in the same technology



Images from: A.La Rosa, "Irradiation induced effects in the FE-I4 front-end chip of the ATLAS IBL detector", IEEE NSS 2016

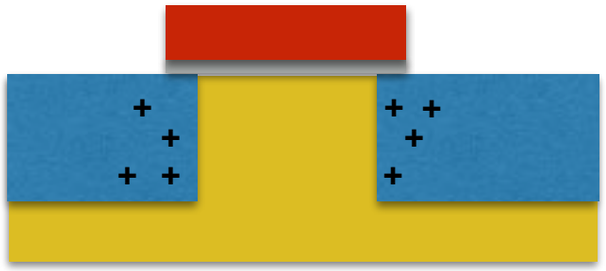
The alternation of irradiation and annealing produces consecutive “bumps” of smaller peak amplitude, suggesting that an attenuation of the problem occurs when sufficiently large TID has accumulated

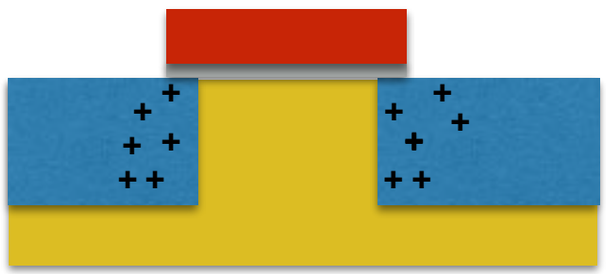


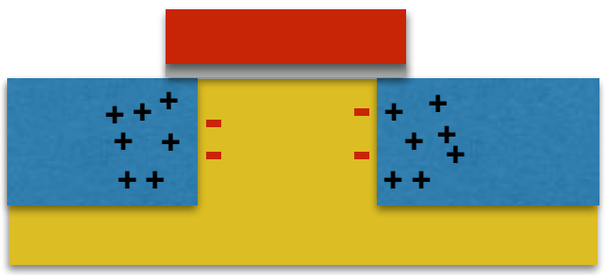
Images from: A.La Rosa, “Irradiation induced effects in the FE-I4 front-end chip of the ATLAS IBL detector”, IEEE NSS 2016

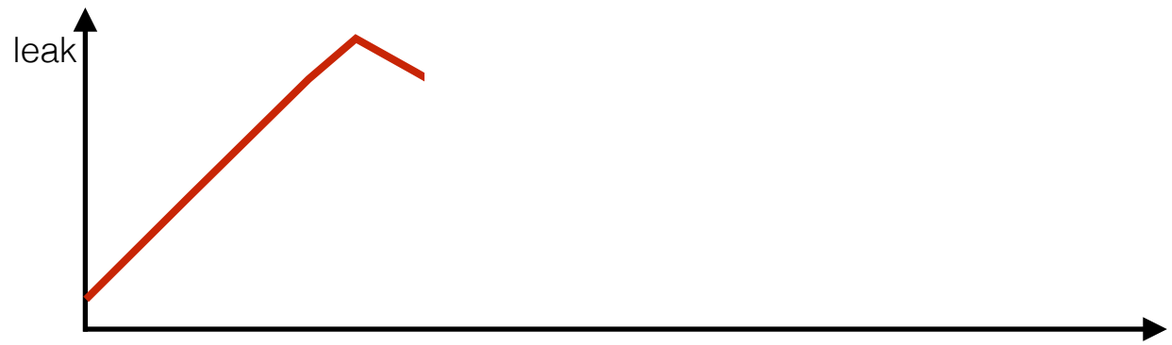
On the basis of our understanding of the mechanisms leading to the leakage current, the following scenario is plausible for discontinuous irradiation tests

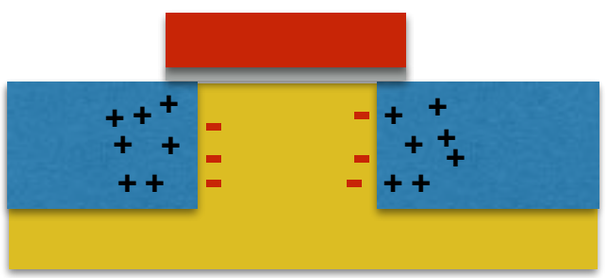
Irradiation

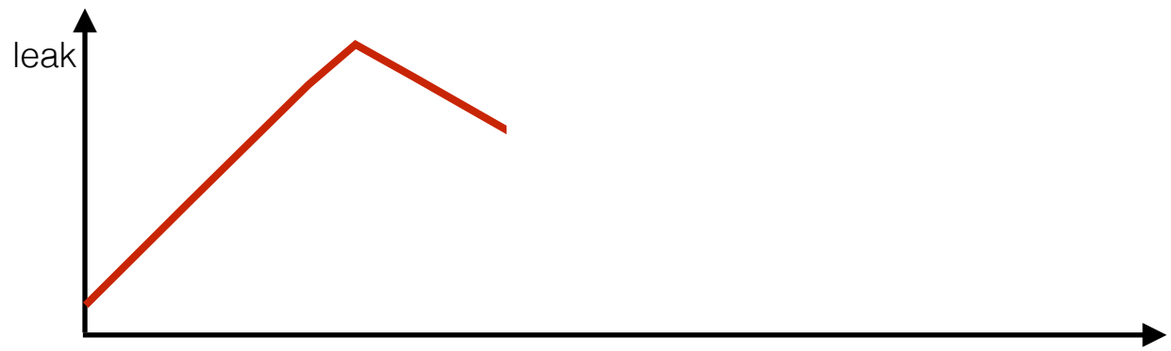




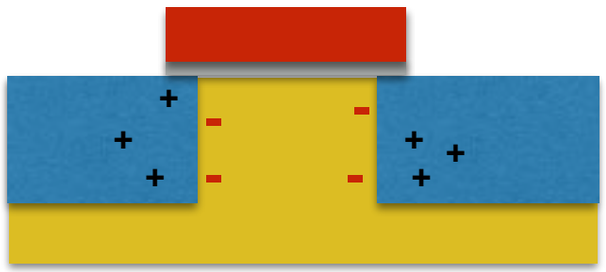


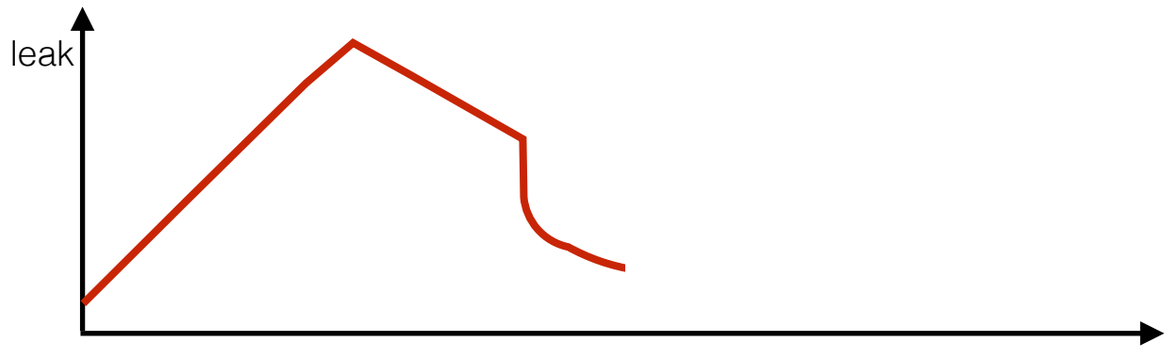




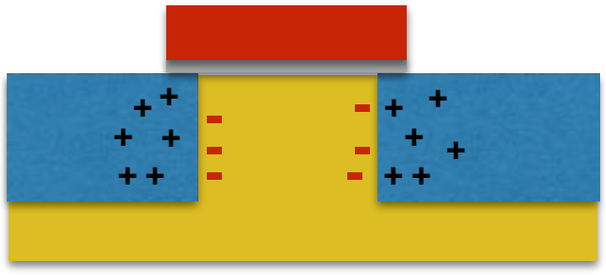


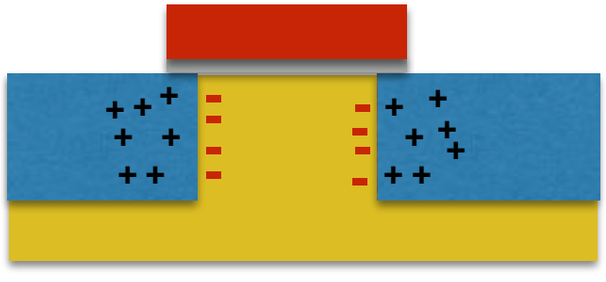
Annealing

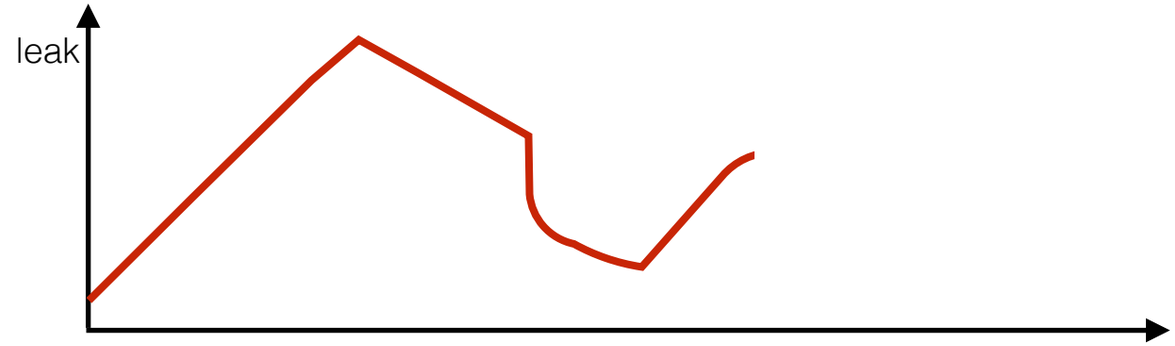


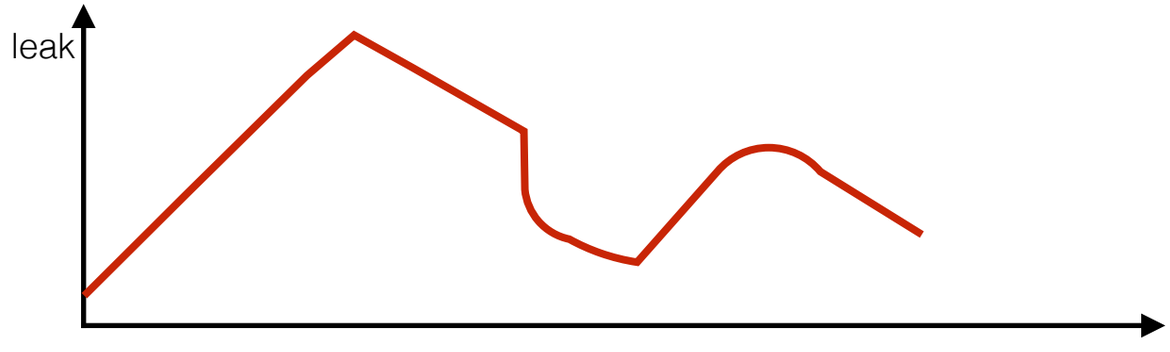


Irradiation









Solution in ATLAS pixels

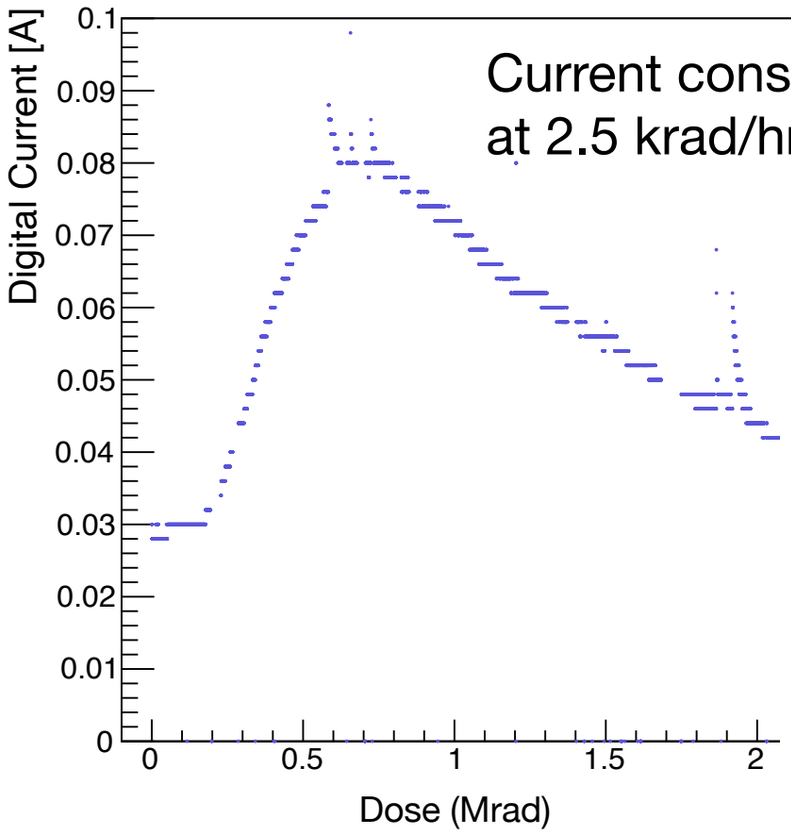
- **rise the temperature of the detector (as much as compatible with safe operation)**
- **patiently wait until the TID brings the chips after the “TID bump”**

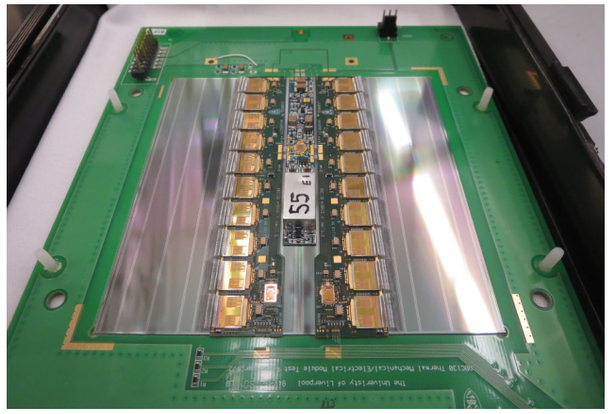
but in general, we can think the accumulation of sufficient TID to be a possible strategy to avoid the appearance of a large “bump” in the current consumption

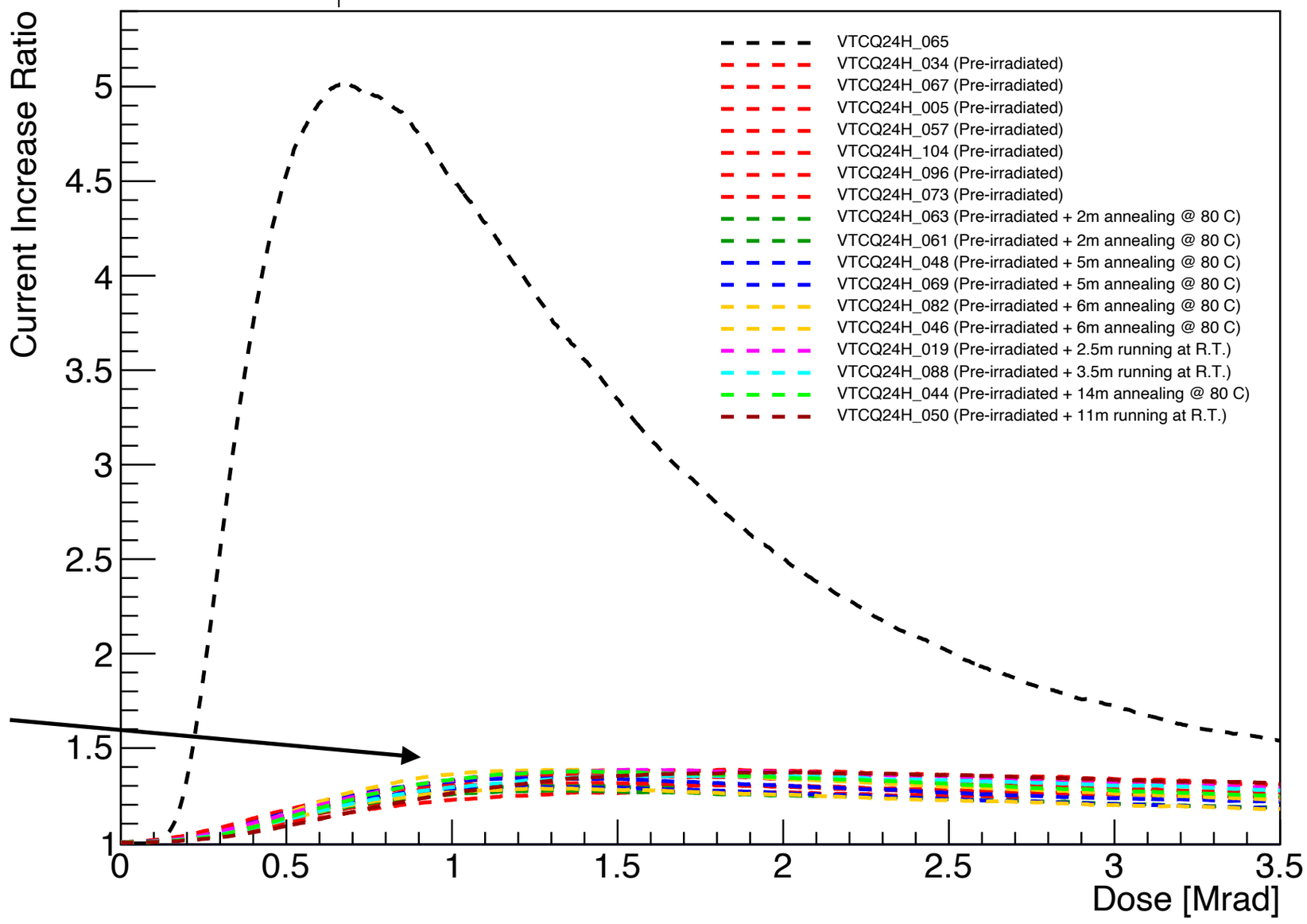
Warning: temperature and dose rate play a key role, and the strategy can only work

IF interface states do not significantly anneal at the operational temperature

Example where the pre-irradiation strategy is used: the ABCstar readout ASIC for the ATLAS HL-LHC inner tracker (strip detector).







Pre-irradiation very significantly reduces the peak of the “bump” AND interface states do not anneal quickly

Images from: L.Poley et al., “The ABC130 barrel module prototyping programme for the ATLAS strip tracker”, 2020 *JINST* **15** P09004

Case study 2

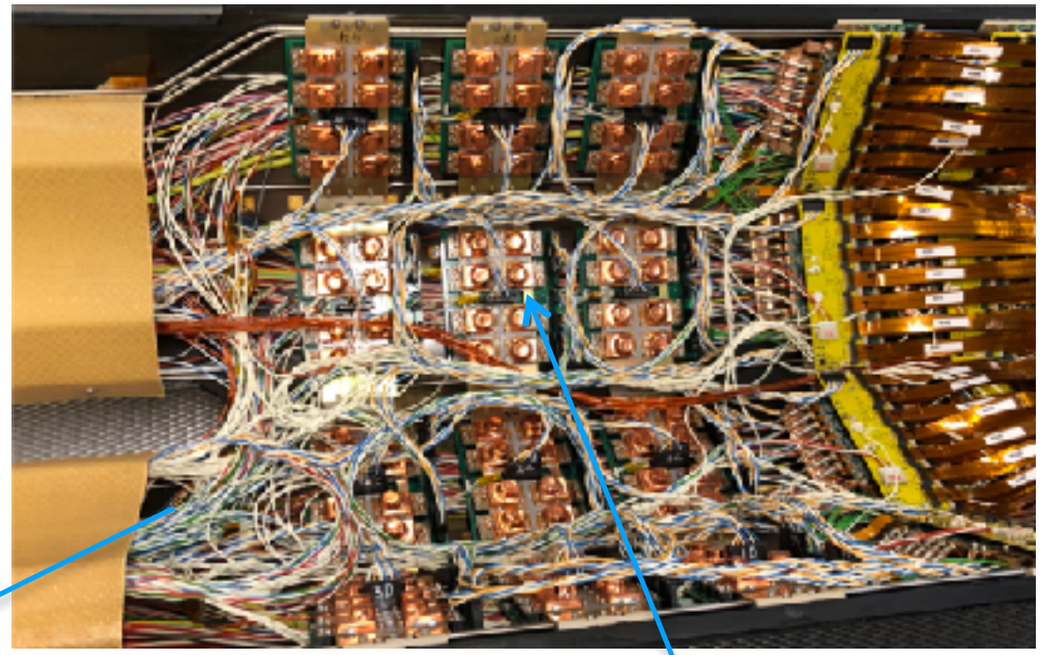
The lonely perpetrator in the DCDC FEAST2 case

How an individual transistor threatened the operation of the CMS pixel detector

Investigation = the act or process of examining a crime, problem, statement, etc. carefully, especially to discover the truth

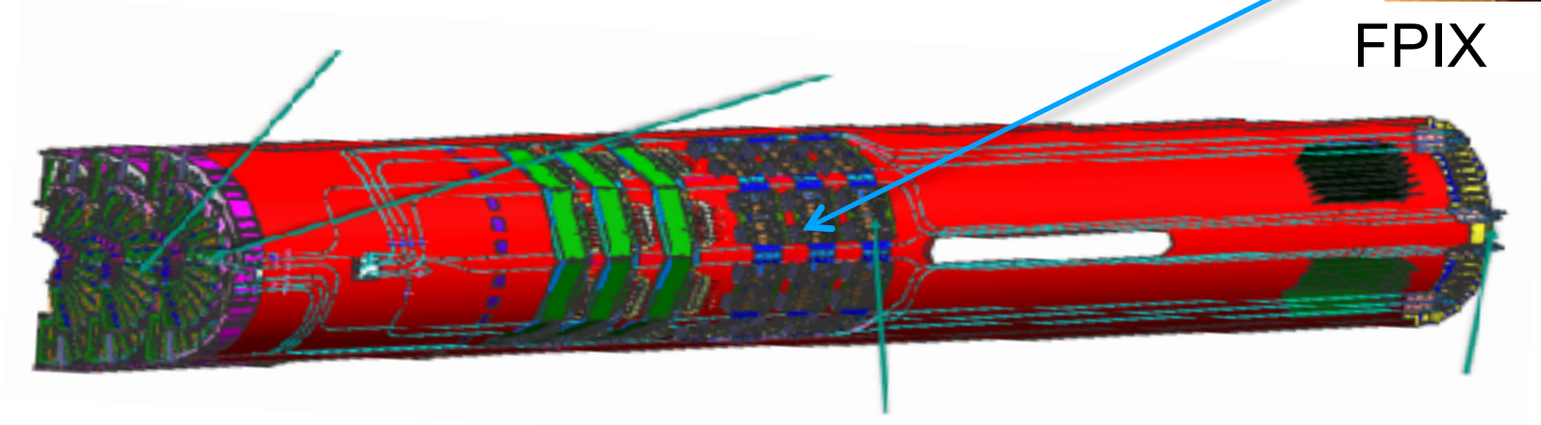
The crime scene

FEAST2 in the CMS pixel detector



FPIX

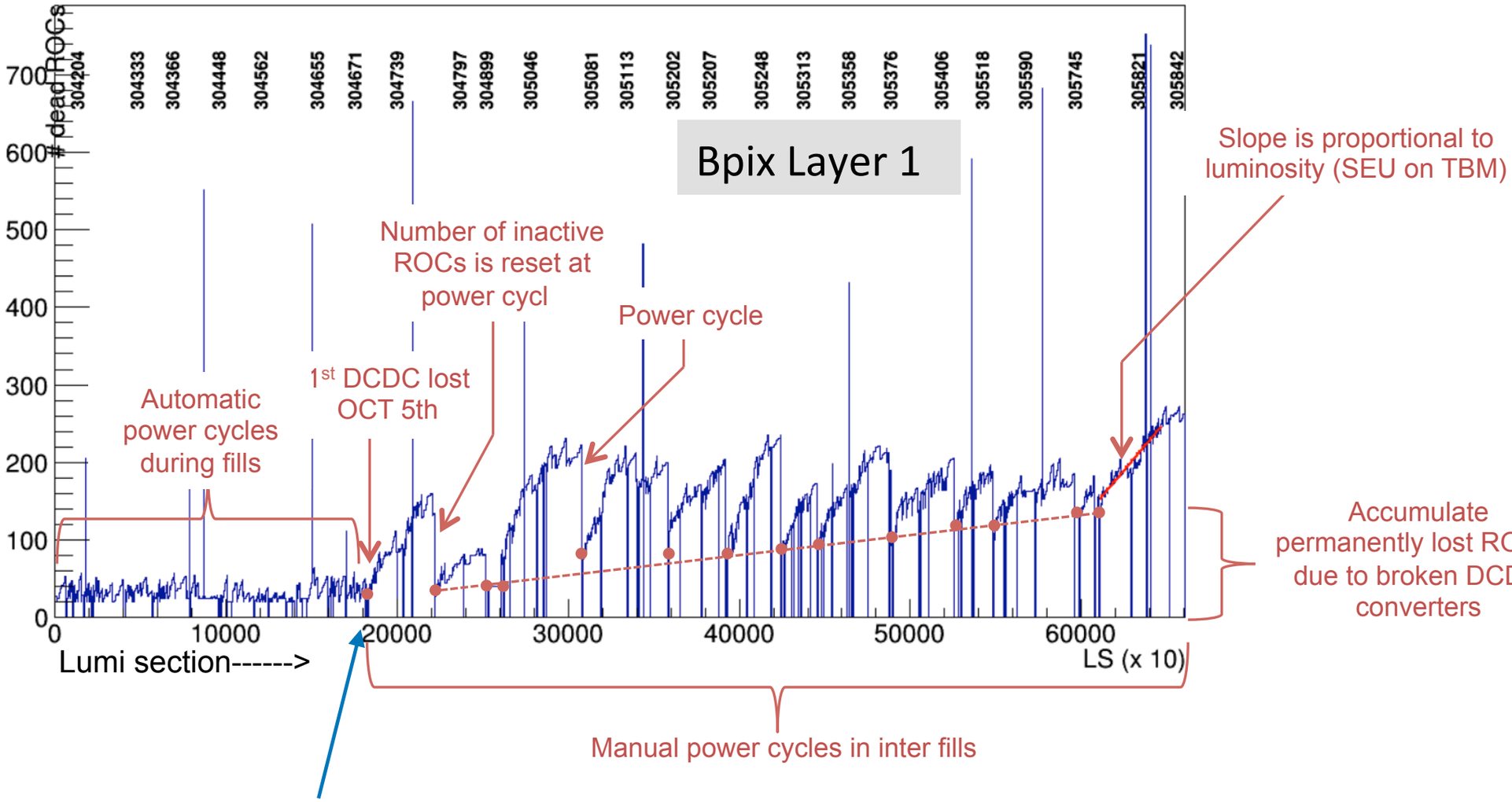
Cooling at -20°C



Bpix DC-DC: radius 240mm, z range 2067- 2430mm from i/p.
Fpix DC-DC: radius 140mm, z range 1315-1530mm from i/p

Witnesses

Failure of FEAST DCDCs in the CMS pixel detector



No correlation with:

- output voltage
- output current
- position in the detector
- anything other than the beam

DCDCs fail during disable/enable cycles

Plan around November 2017

Rest of 2017 Physics Run

Nothing can be done.
Accept loss of modules

YETS 17-18

Request longer Year-End Stop
Open the detector
Extract all DCDC modules
Replace (all?) modules (fuse changed)

2018 Physics Run

Find a patch ensuring
data taking

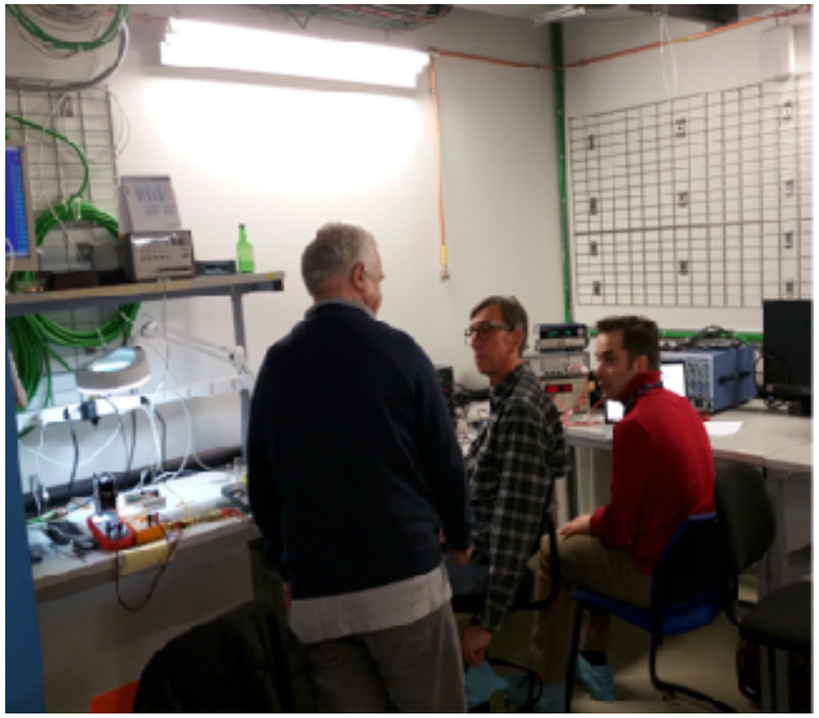
LS2

Solve the problem
for the long term

"At this pace, game over
for CMS around May 2018"

The autopsy

YETS 17-18: Merry Christmas!



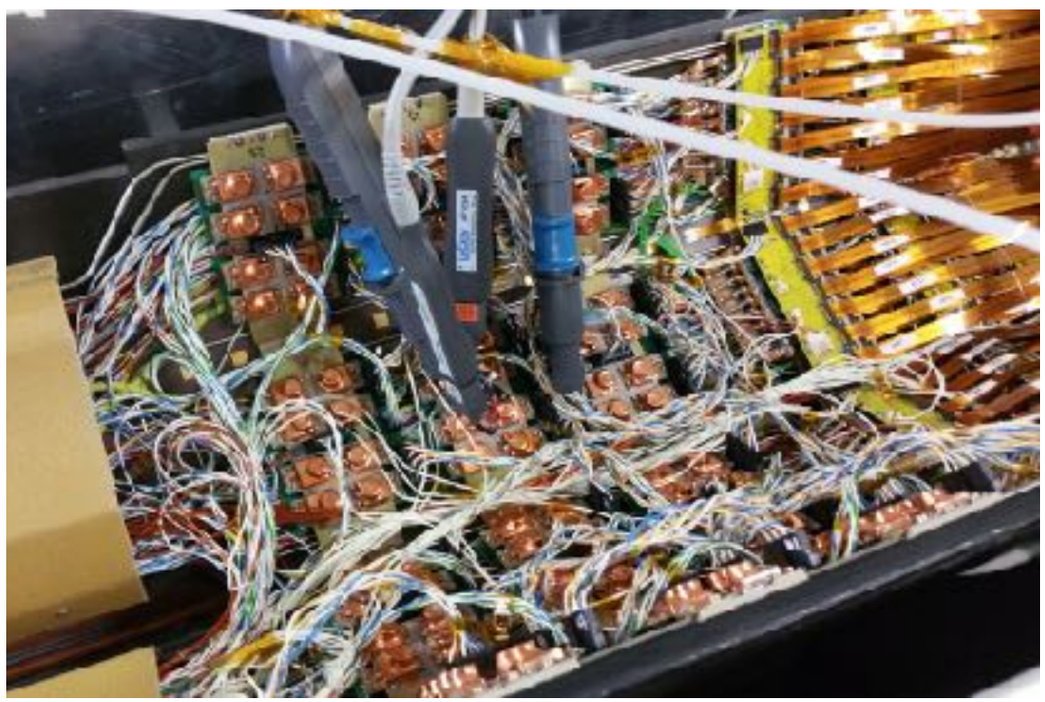


Photo memories from the 2017 Christmas Break

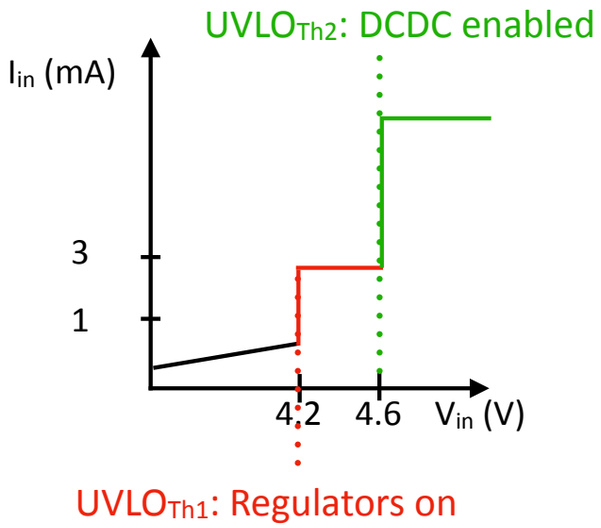
FEAST2 modules in the CMS experiment were found to present 2 distinct types of damage

- “Broken” samples failed to provide any output voltage
- “High-current” samples were perfectly functional, but were found to have an excessive current below UVLO

Perfectly working in the system but found to have anomalous current when tested

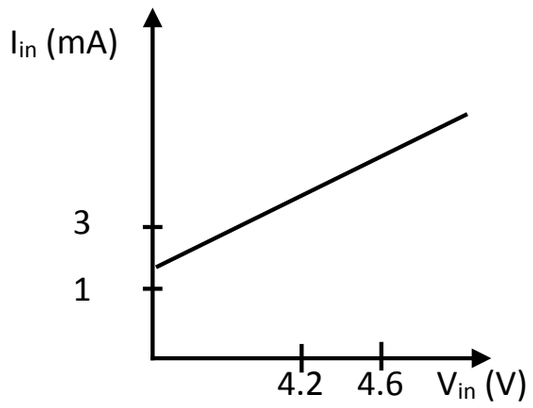
	Pixel Names	Number of Converters	Tested Broken	Tested working with High Current	Tested working with normal current	BROKEN	HIGH CURRENT
		TOTAL	"BROKEN"	"HIGH CURRENT"	"GOOD"	% with respect to total	% with respect to total working
BPIX (+Z, Near)	BPIX-BpI	208	4	48	156	1.9	23.5
BPIX (-Z, Near)	BPIX-BmI	208	10	48	150	4.8	24.2
BPIX (+Z, Far)	BPIX-BpO	208	13	70	125	6.3	35.9
BPIX (-Z, Far)	BPIX-BmO	208	11	70	127	5.3	35.5
FPIX (+Z, Near)	FPIX-BpI	96	7	41	48	7.3	46.1
FPIX (-Z, Near)	FPIX-BmI	96	7	34	55	7.3	38.2
FPIX (+Z, Far)	FPIX-BpO	96	9	23	64	9.4	26.4
FPIX (-Z, Far)	FPIX-BmO	96	6	22	68	6.3	24.4
BPIX - not connected to modules		32	2	8	22	6.3	26.7

“Good”



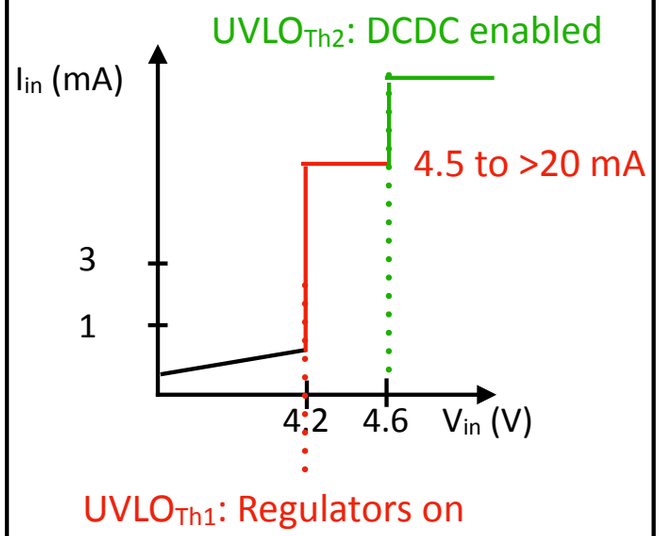
Perfectly working in the experiment

“Broken”



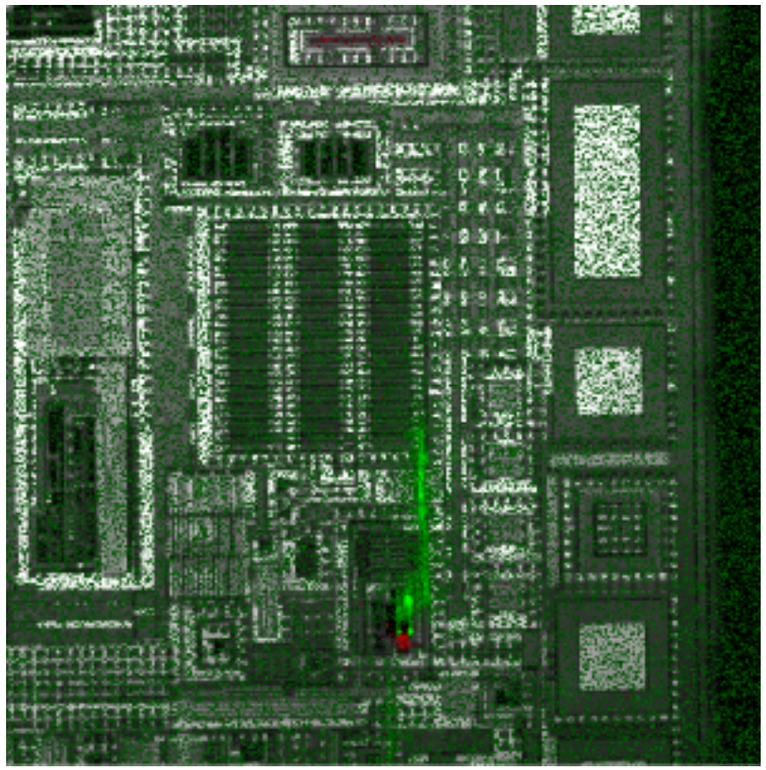
Failed in the experiment

“High current”

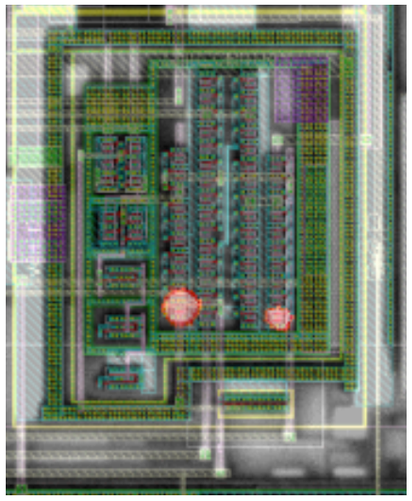


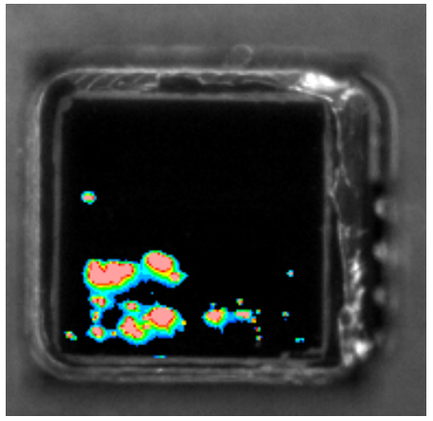
Perfectly working in the experiment

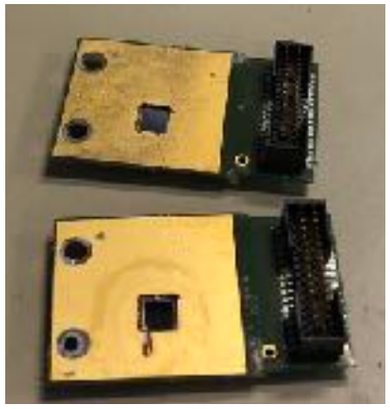
Failure Analysis (FA) with emission microscopy and Optical Beam Induced Resistance Change (OBIRCH) at MASER (NL)

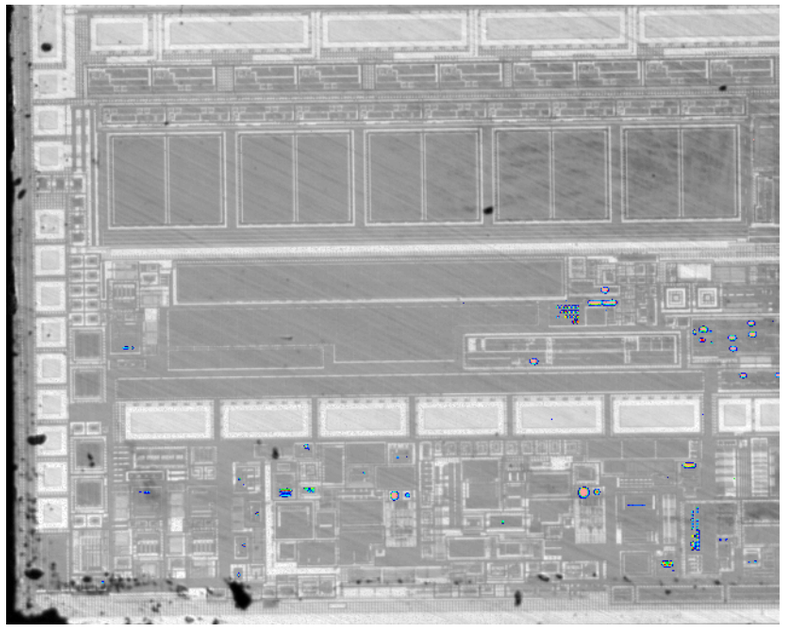


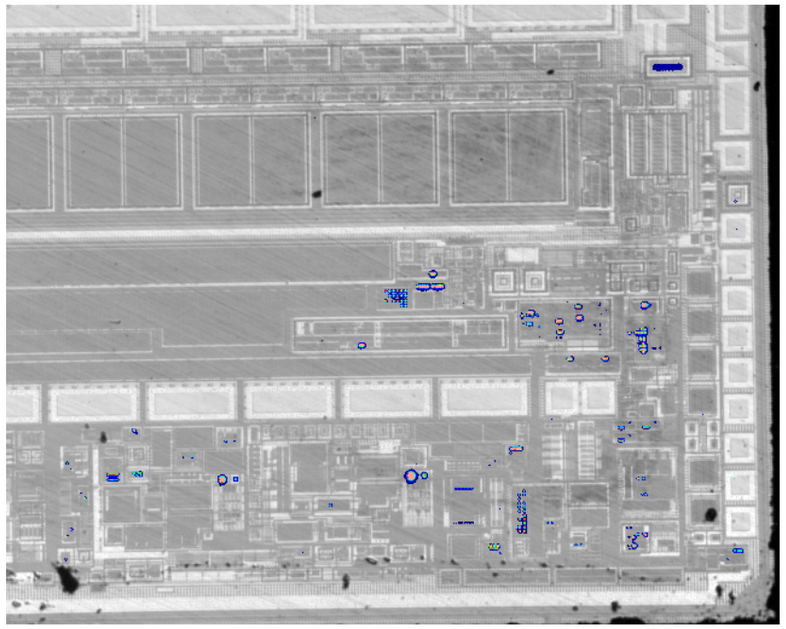
During OBIRCH a laser beam selectively illuminates the metal lines, altering their resistance. The consequent input current change is measured, allowing the mapping of current paths. In broken FEAST2 samples, current flows to the clamp transistors.





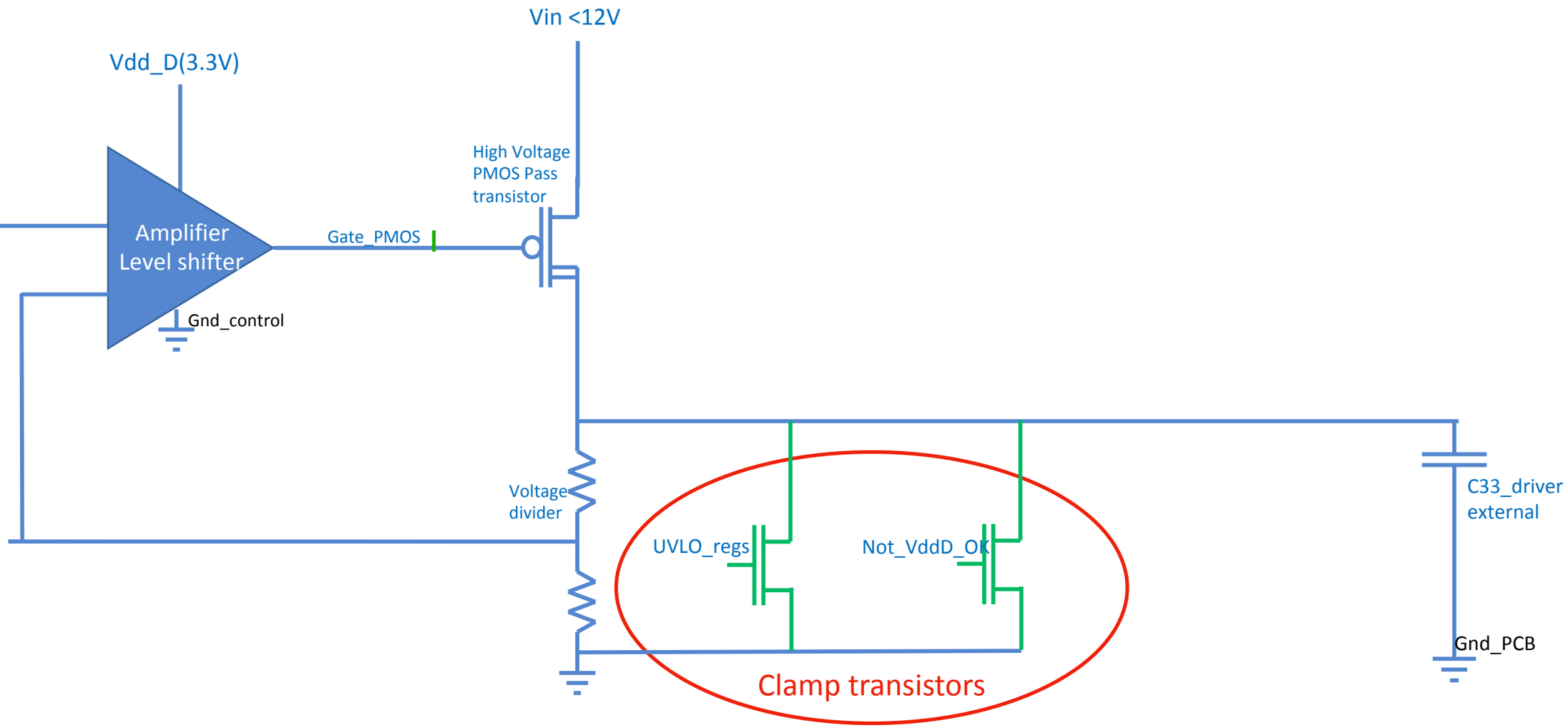






Emission images are based on the detection of photons generated from hot carriers (therefore only conducting NMOS transistors are well visible). "Broken" or "High-current" FEAST2 samples showed different current paths.

Observations match the hypothesis that one of the two on-chip clamp transistors is damaged



The motive

Why the clamp transistor(s) is(are) damaged?

Flawed ASICs?

Flawed PCBs?

Radiation in ASIC?

EM noise?

Radiation in package?

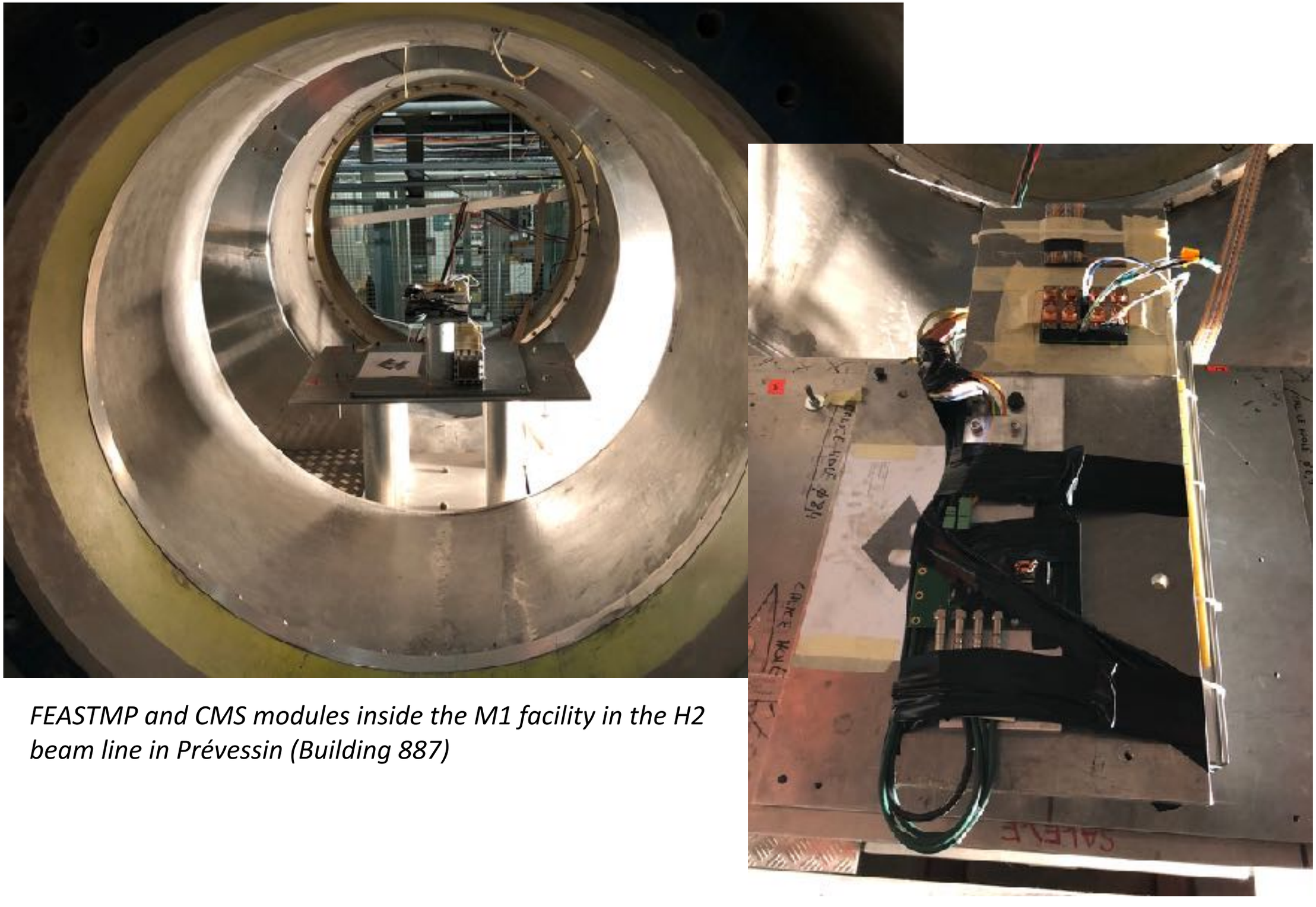
Environmental conditions?

Electrical stress?

Combination of any of the above??

Environmental conditions?

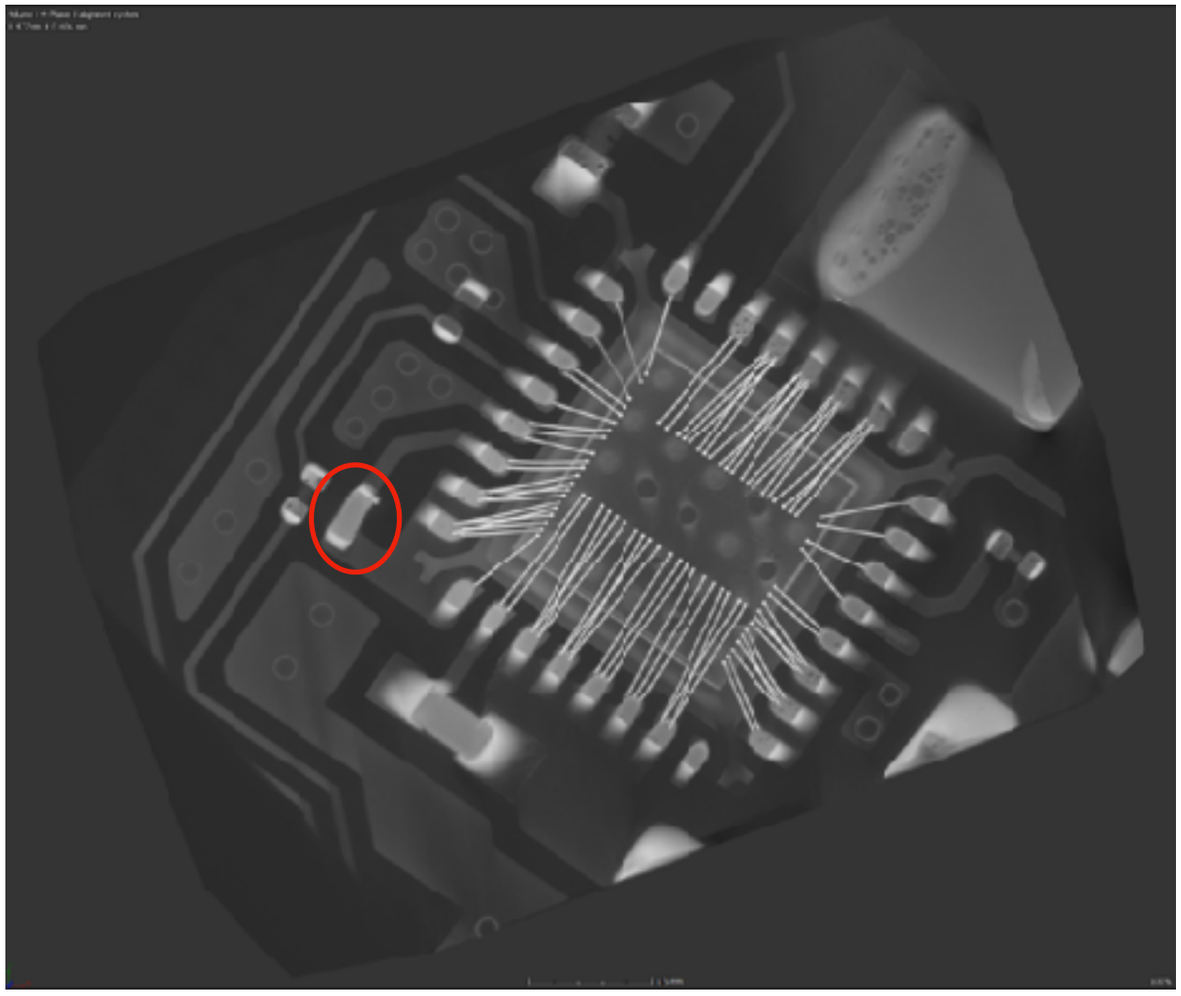
Test in a 3T magnetic field revealed no problem



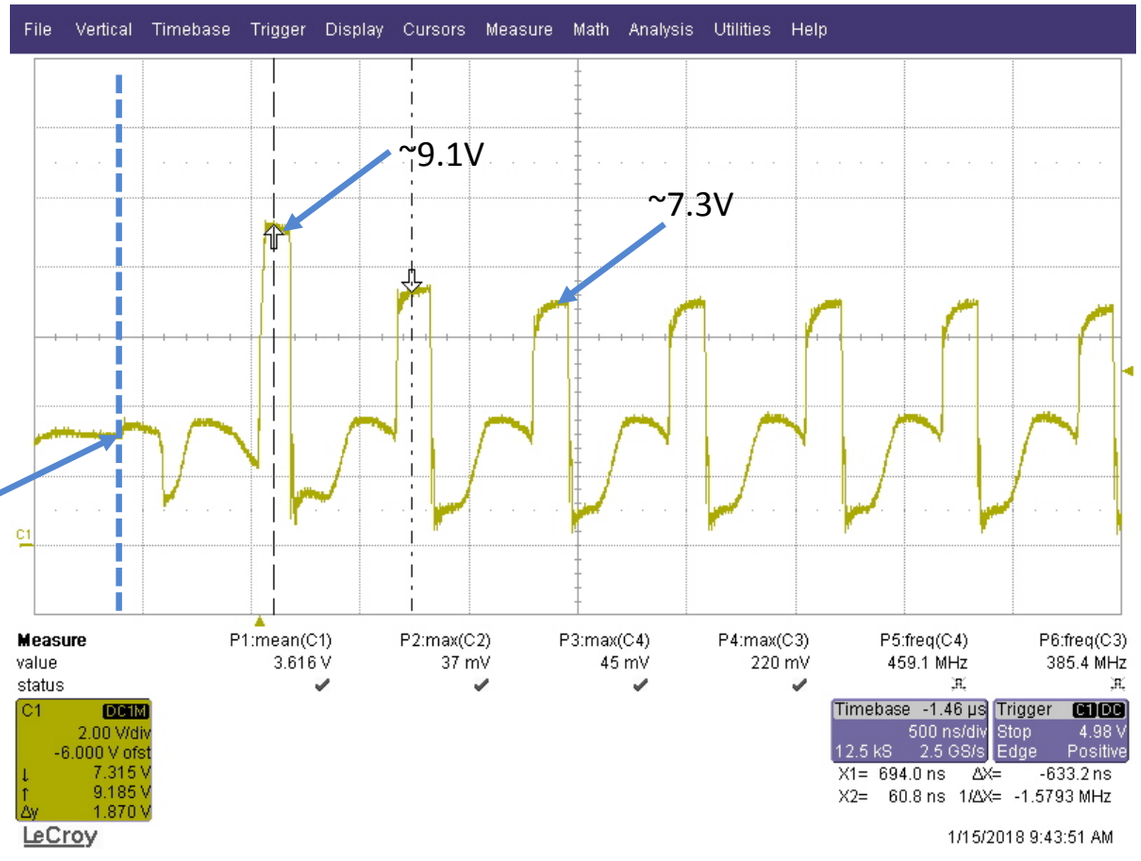
FEASTMP and CMS modules inside the M1 facility in the H2 beam line in Prévessin (Building 887)

Flawed PCBs?

Faulty capacitor, or intermittent contacts of the capacitor in the PCB generated a stress that produced somewhat similar damage



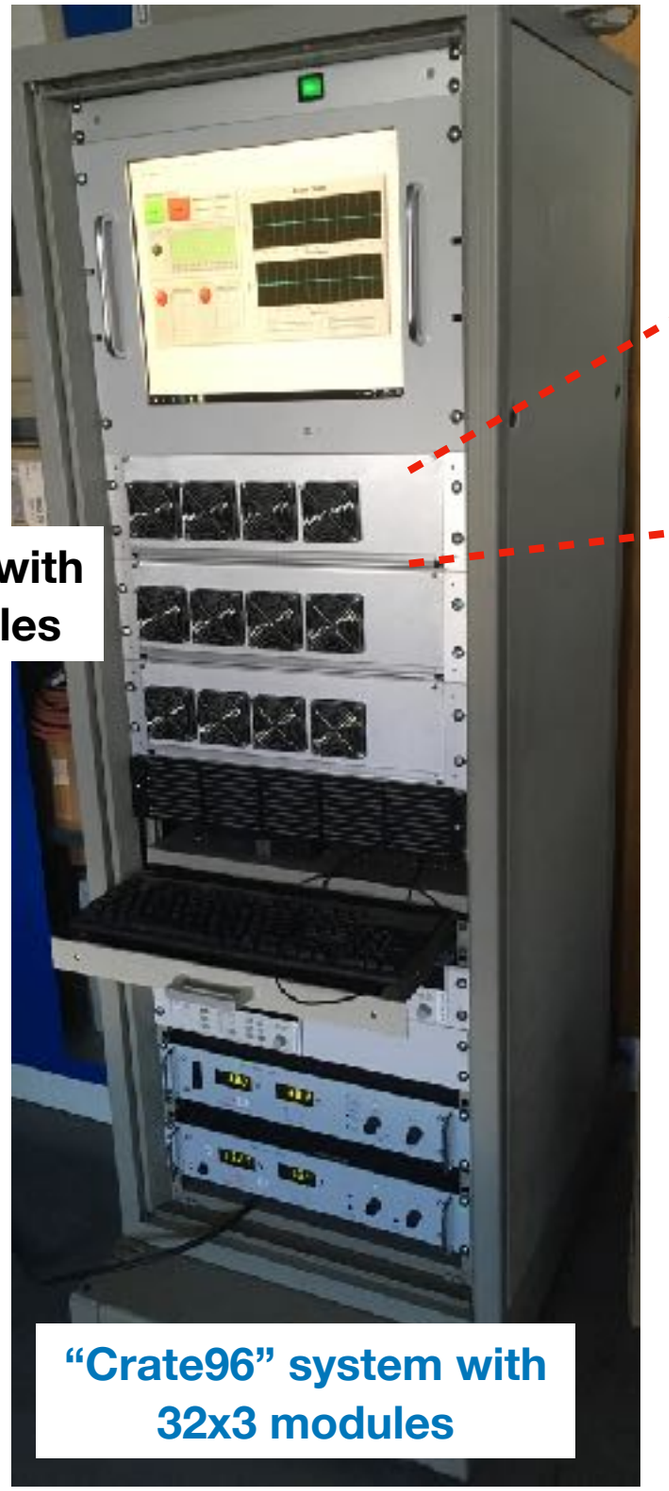
3D X-ray imaging of the module to inspect the quality of the soldering of the capacitor to the PCB



Waveform of the V33Dr node when the capacitance has intermittent contacts to the PCB

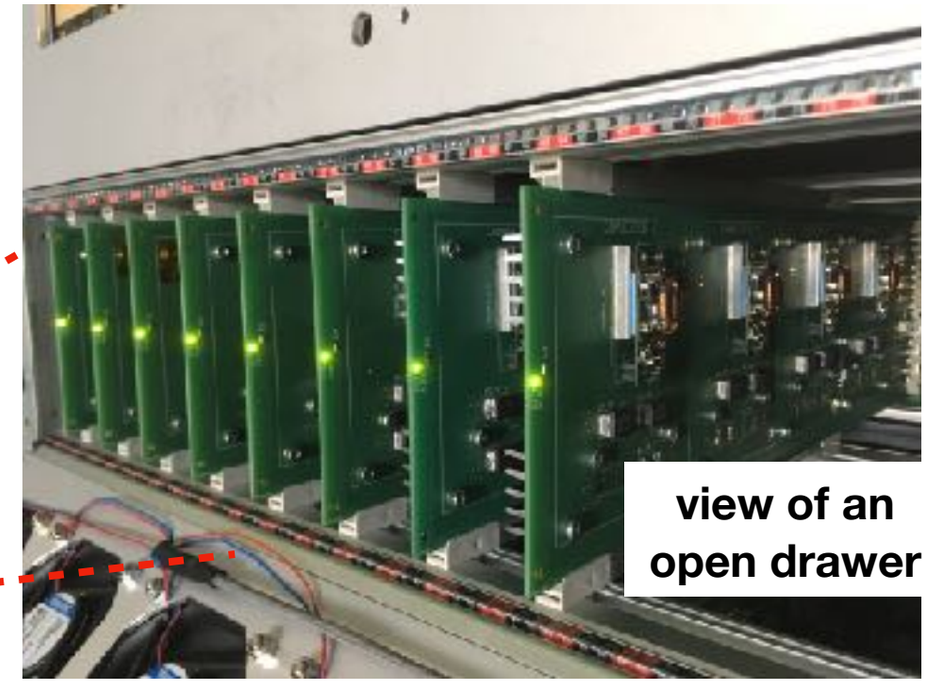
Electrical stress?

Long-term ageing tests on 124 converters did not reveal problems with FEAST2 ASICs

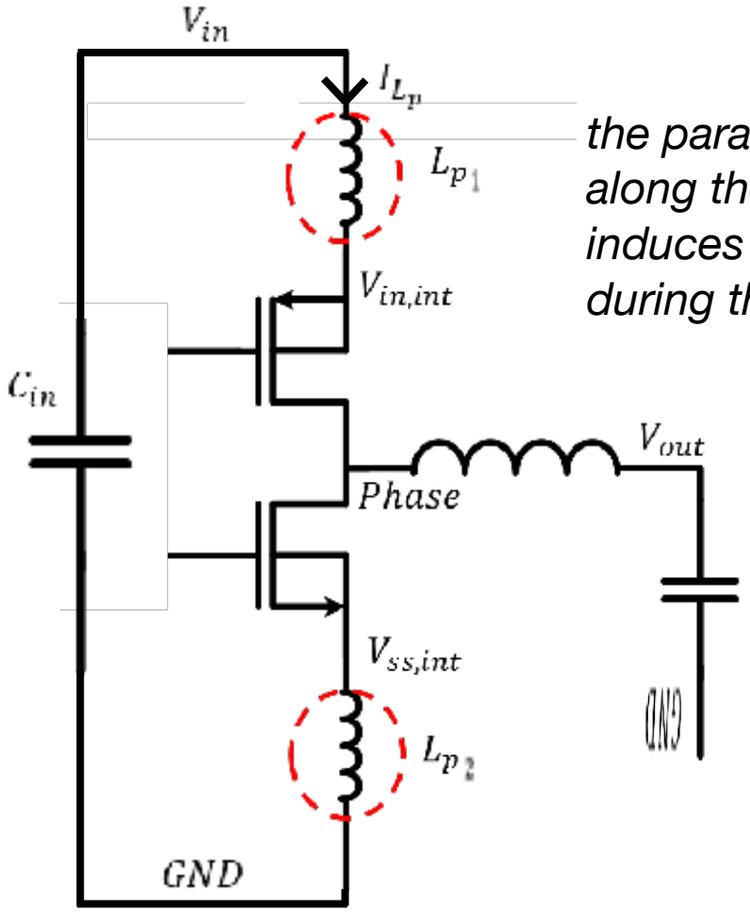


3 drawers with 8x4 modules

“Crate96” system with 32x3 modules



view of an open drawer

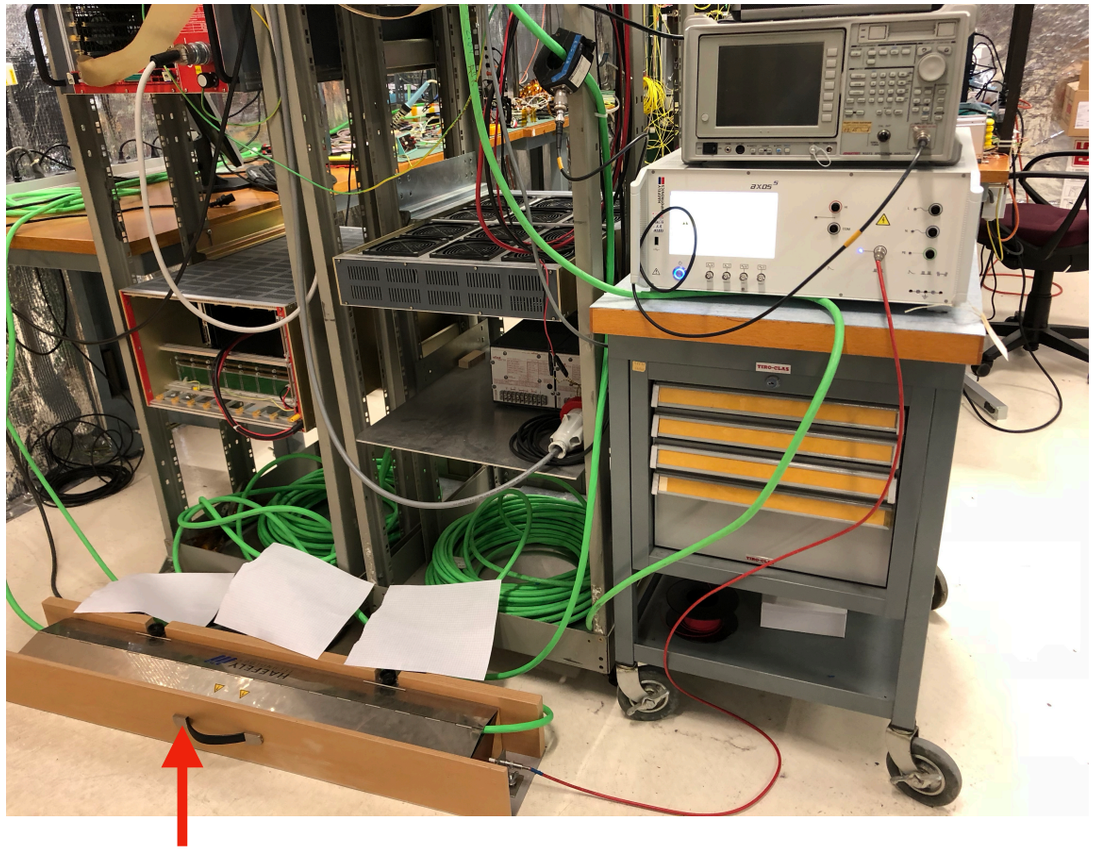


the parasitic inductance along the current path induces over-voltages during the commutations

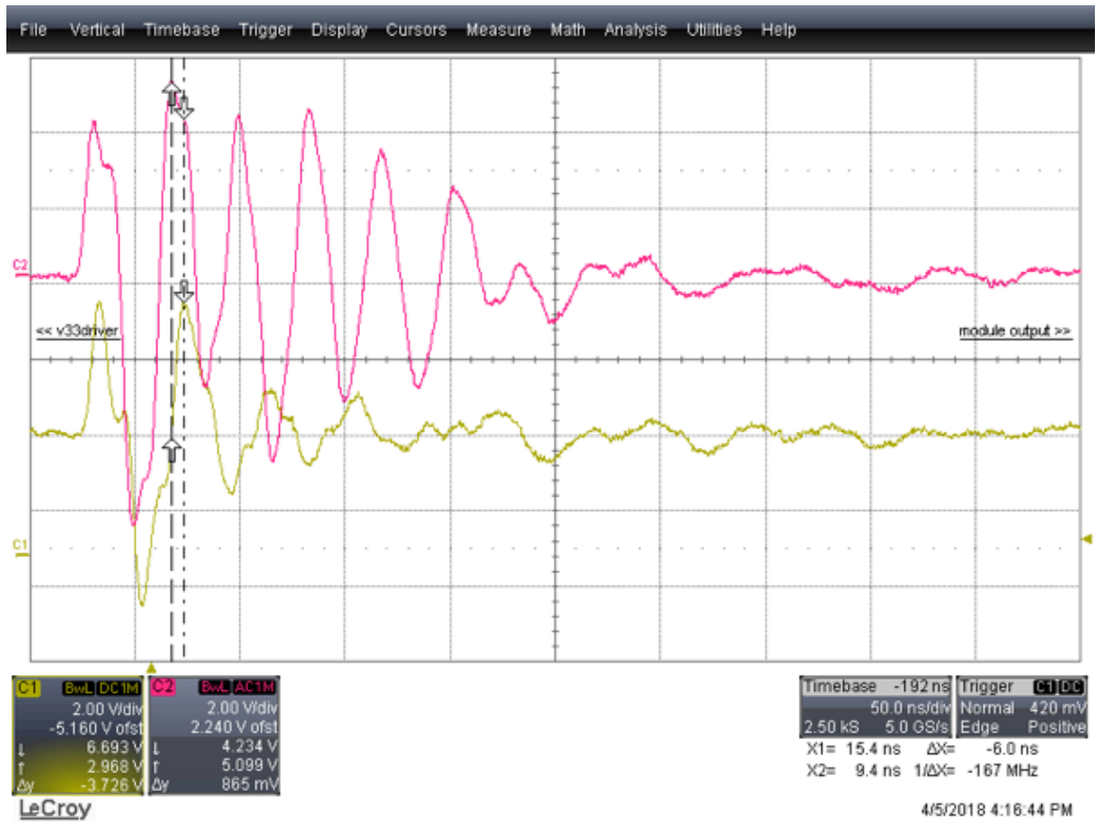
EM noise? Environmental conditions?

Injection of EM noise by capacitive coupling to the input/output and signal lines. The converter appears to be very resilient

Led by F. Szoncso and D. Valuch



Capacitive high-frequency coupler used on the input bus line



AC-observation of the effect of a 3kV (!) pulse with 50ns duration on Vin and V33Dr. The peak is several V above the DC (V33Dr reaches 8V)!

EM noise? Environmental conditions?

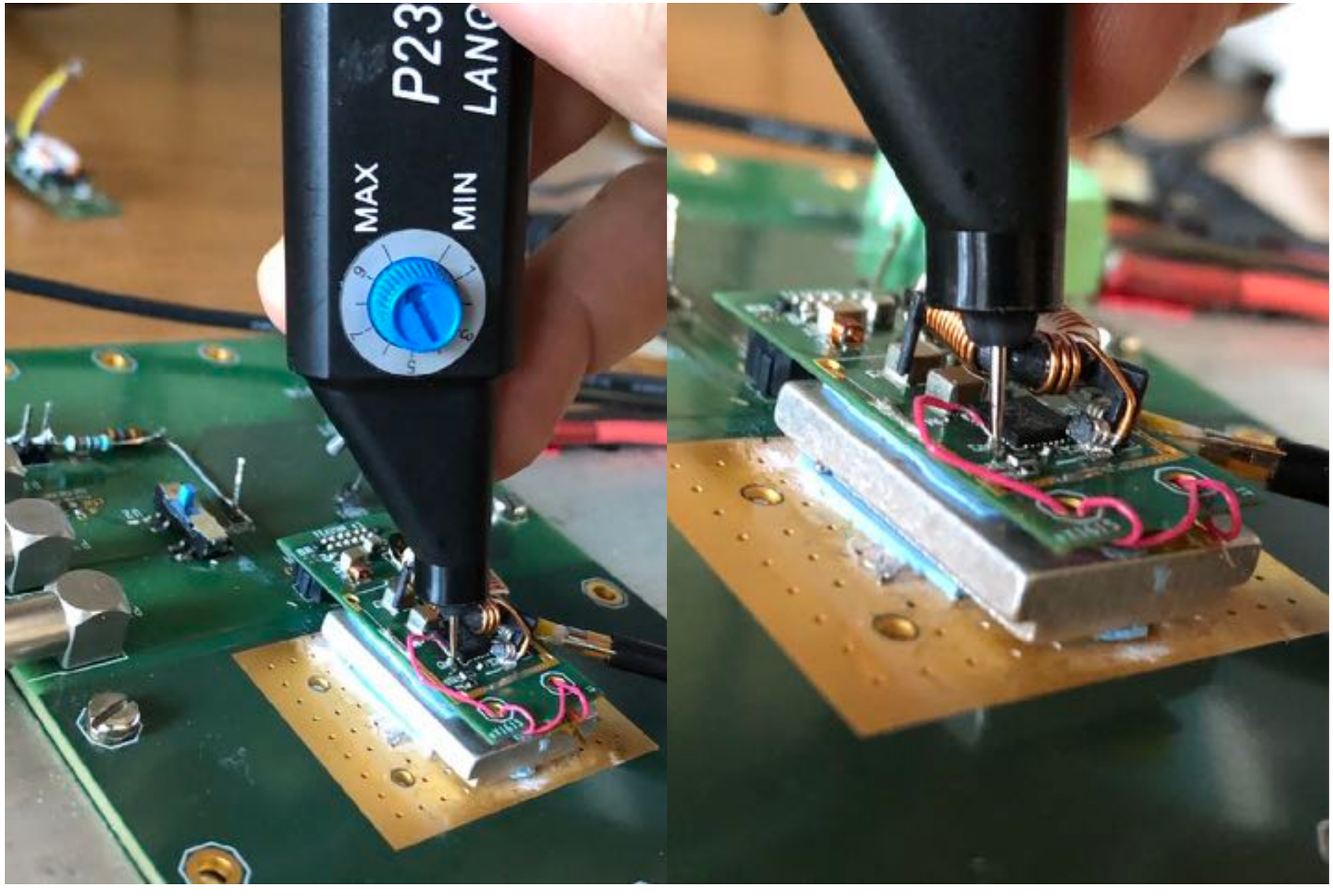
High-frequency, large power RF noise injection could produce damage with different signature

Led by F. Szoncso and D. Valuch

High frequency (GHz) and high power transient pulses are injected via an antenna in a special chamber in CERN Prévessin. At very large power, the ASIC can be damaged but the signature is different than in samples failing in CMS. Coupling is through the long enable line.

EM noise? Environmental conditions?

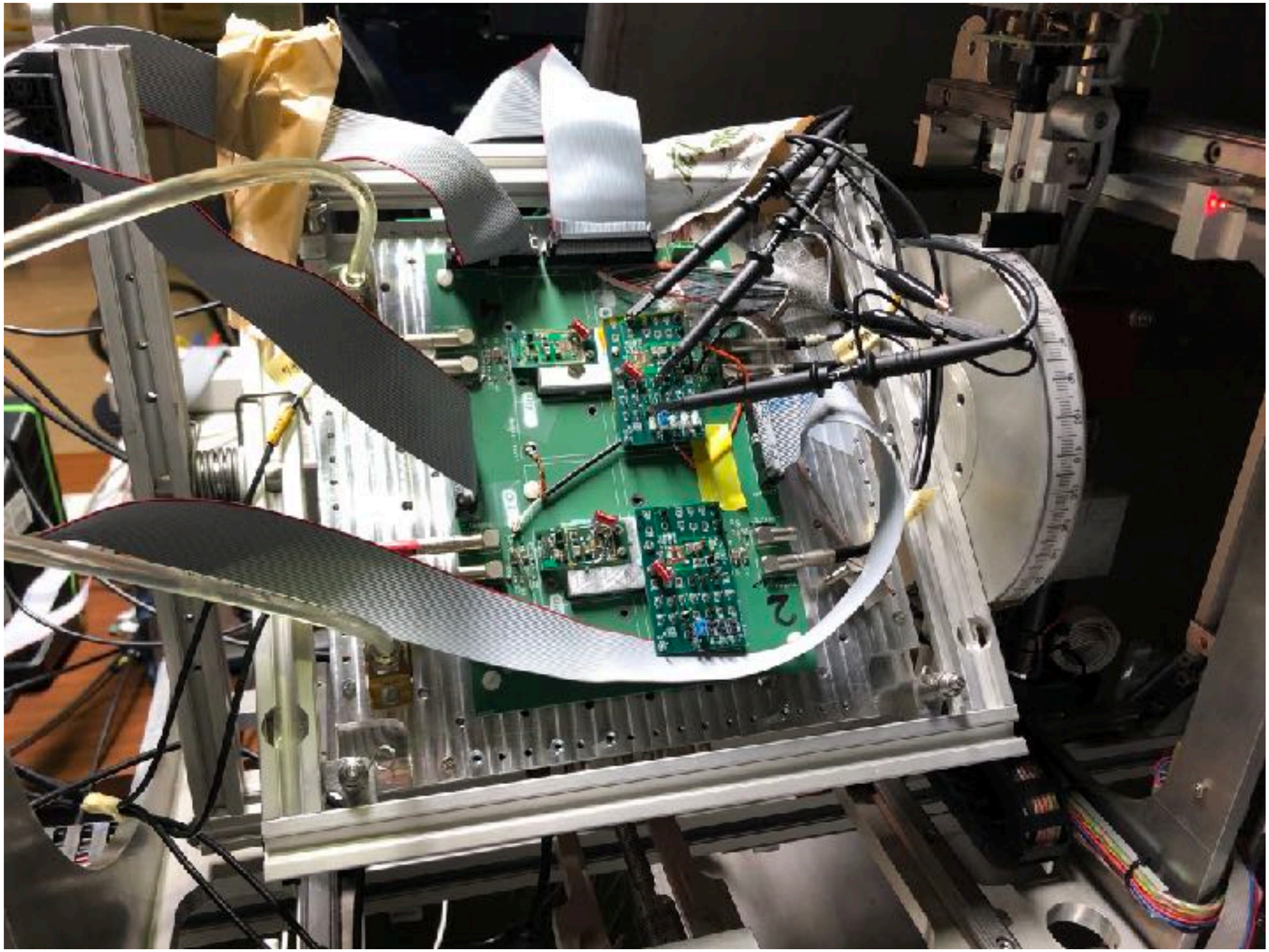
Stress tests with an ESD gun (1.2kV pulses) could produce somewhat similar damage - but the energy injected needs to be really large



An ESD gun is used to inject a discharge to the different pins of the FEAST2 package.
To produce any damage, a visible spark has to be produced.

Radiation in ASIC?

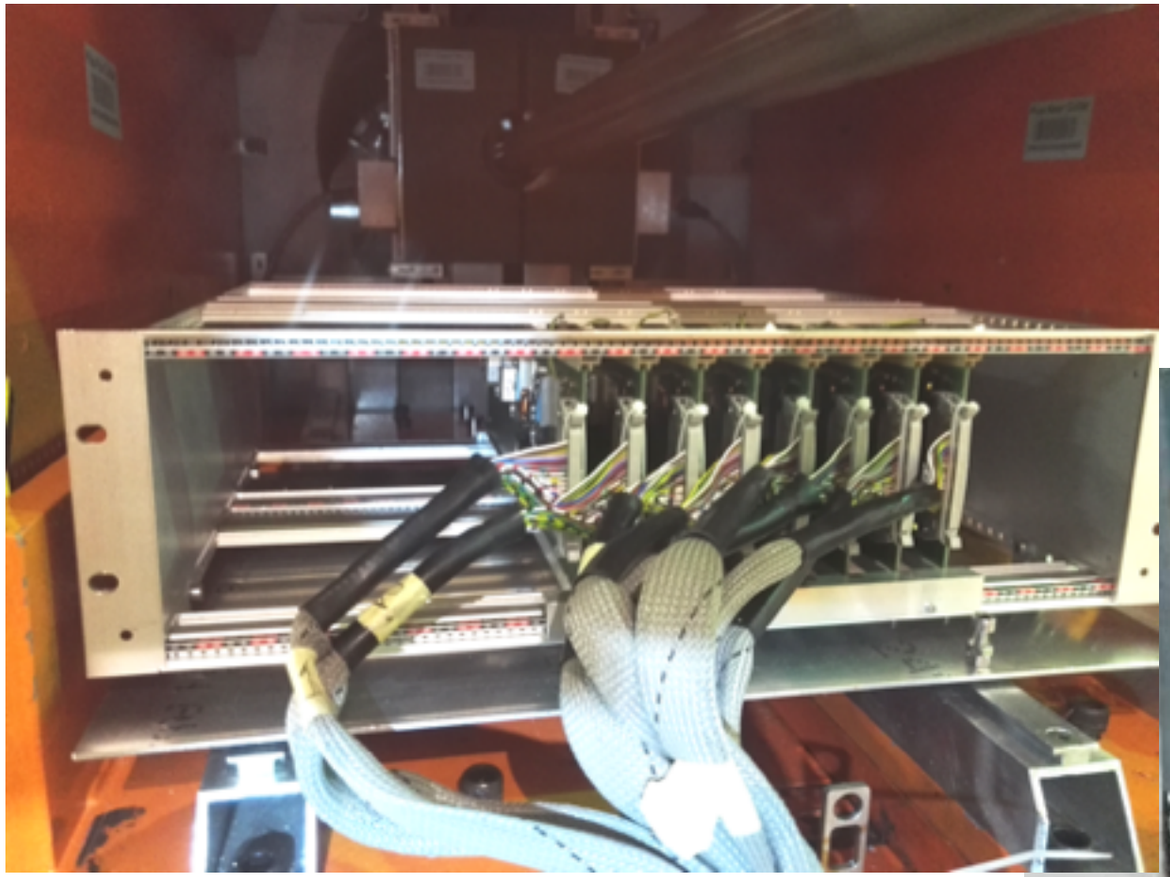
SEE Heavy Ion irradiation on samples pre-exposed to X-rays, Protons and Neutrons did not show any sign of damage

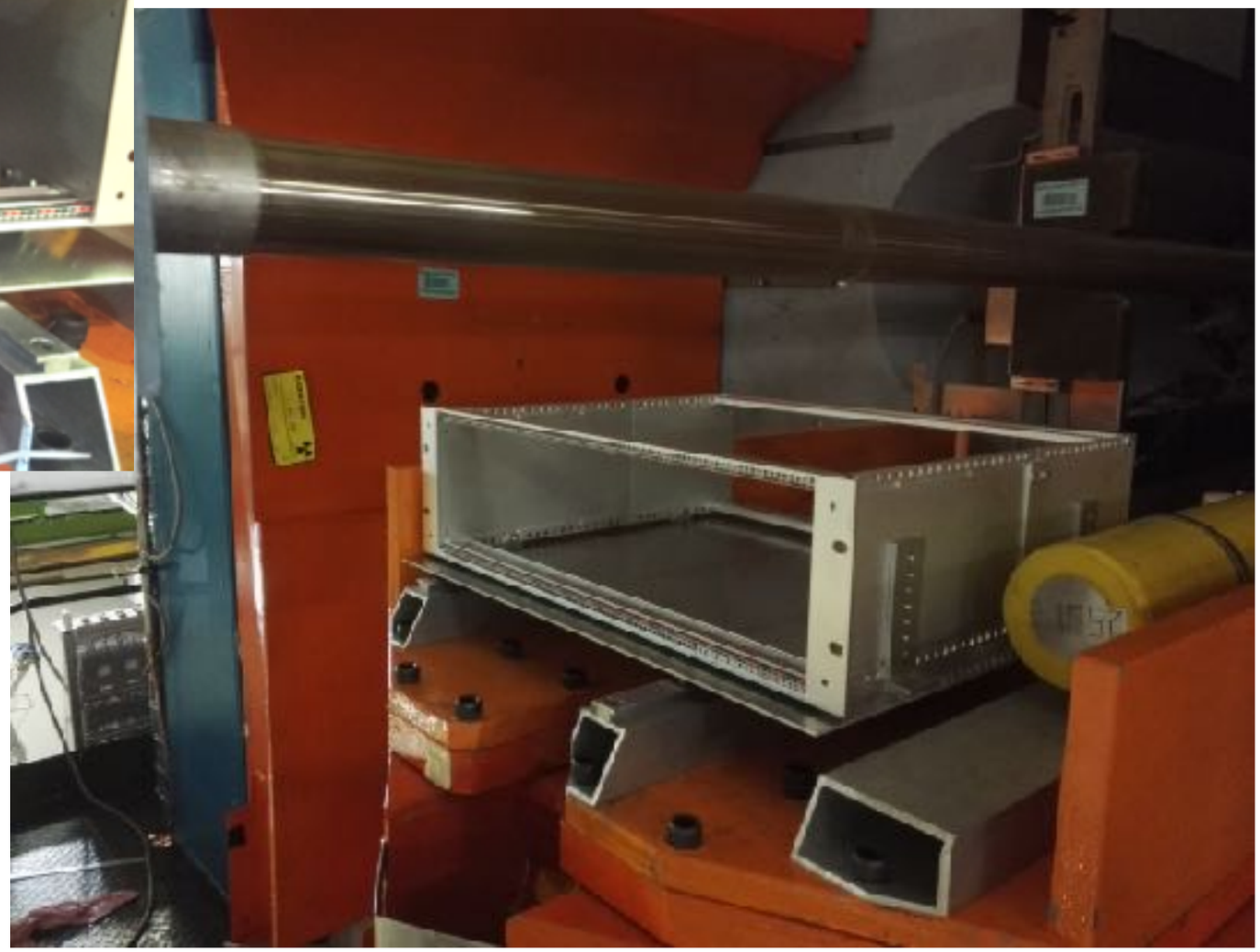


4 modules prepared on a motherboard are placed inside the irradiation chamber where they will be exposed to a Heavy Ion beam. The FEAST2 chips were previously irradiated with X-rays, 230MeV protons or neutrons from a reactor.

Radiation in ASIC? Environmental conditions?

Exposure of 32 FEAST2 in the CMS Castor Table was meant to reproduce some of the environmental conditions (proximity to the beam line, EM environment, radiation environment)





32 sample DCDC modules, both FEASTMP and CMS modules, are exposed and constantly monitored in the CMS Castor Table during the 2018 run.

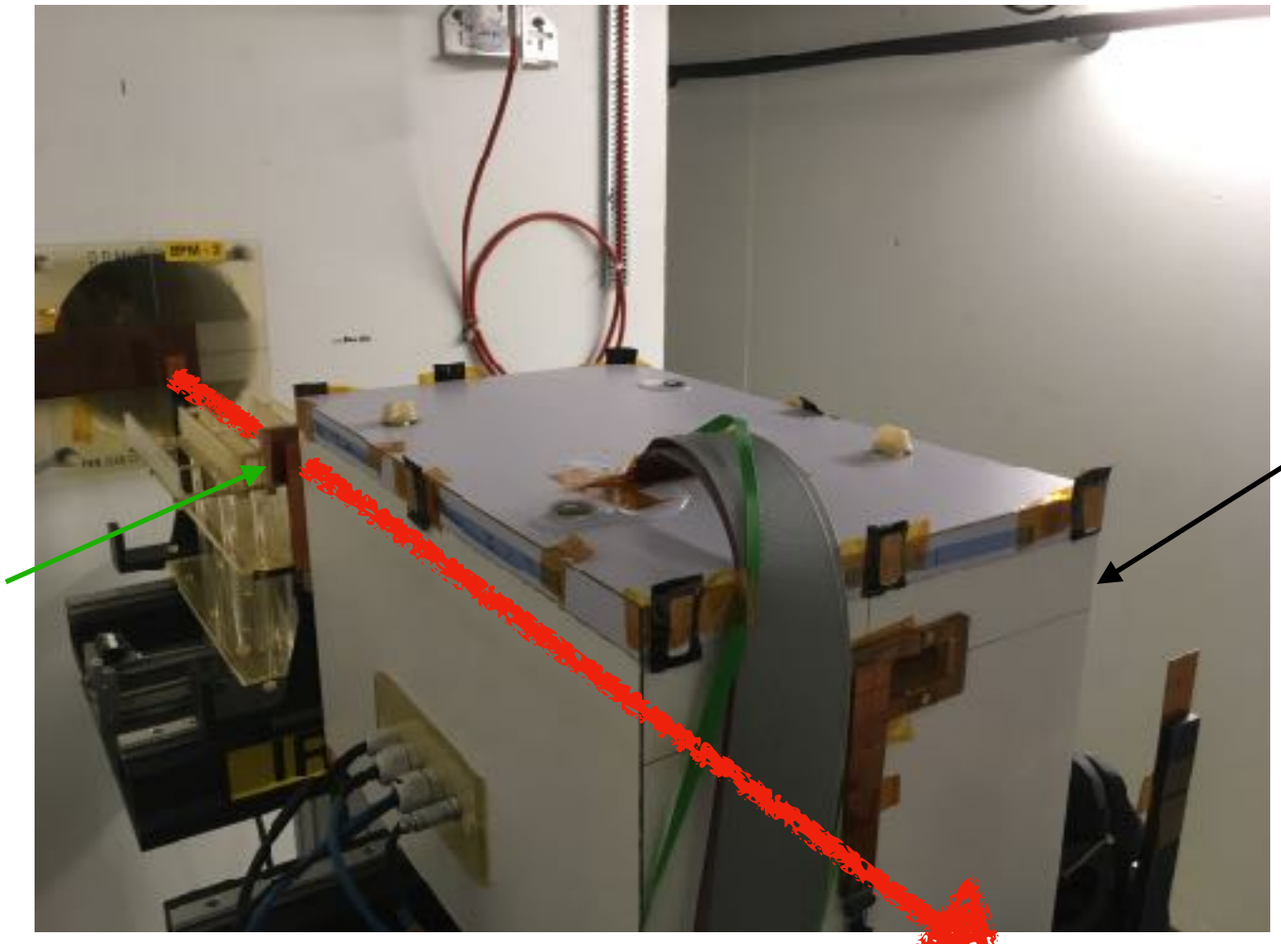
Radiation in ASIC? **Environmental conditions?** **EM noise?**

Two irradiation runs at the CERN IRRAD facility were instrumental in understanding the origin of the damage

Exposure of 32 FEAST2 at -25°C at the CERN IRRAD facility

The facility run in a purposely modified configuration to expose the converters in a mixed field:

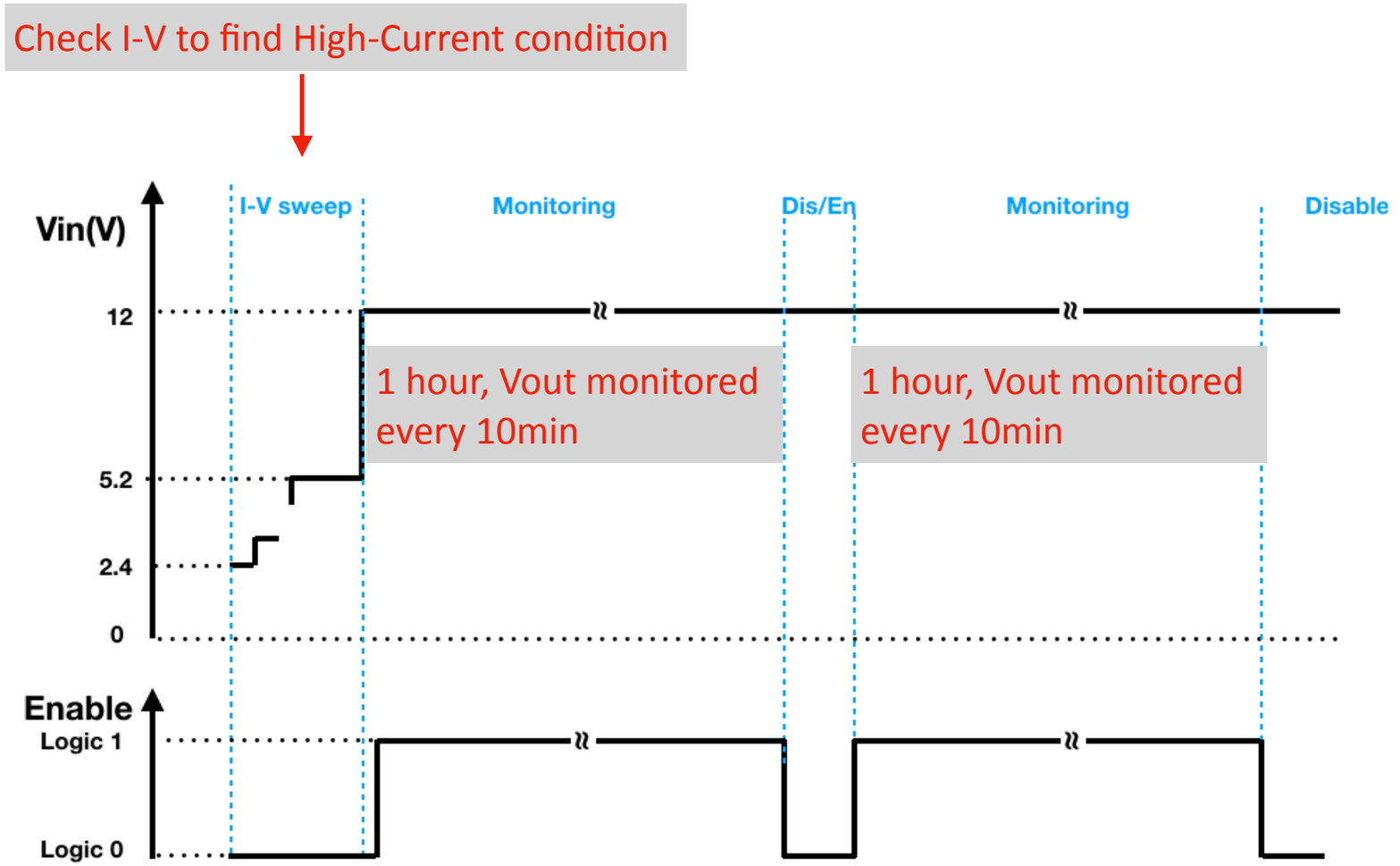
MANY THANKS to the IRRAD TEAM!



32 samples, both FEASTMP and CMS modules, are exposed and constantly monitored in a cold box (-25°C) in the CERN IRRAD facility (May 2018).

32 modules inside the cold box

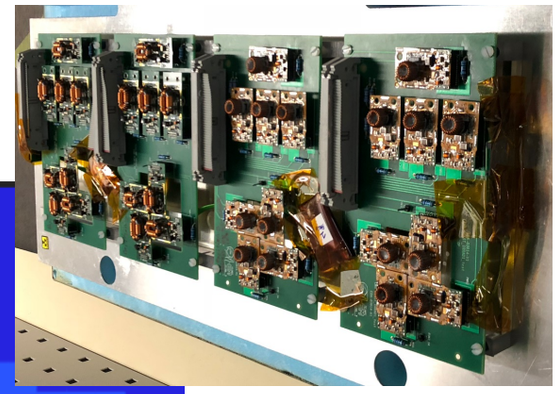
A specific bias and control sequence was used during the exposure

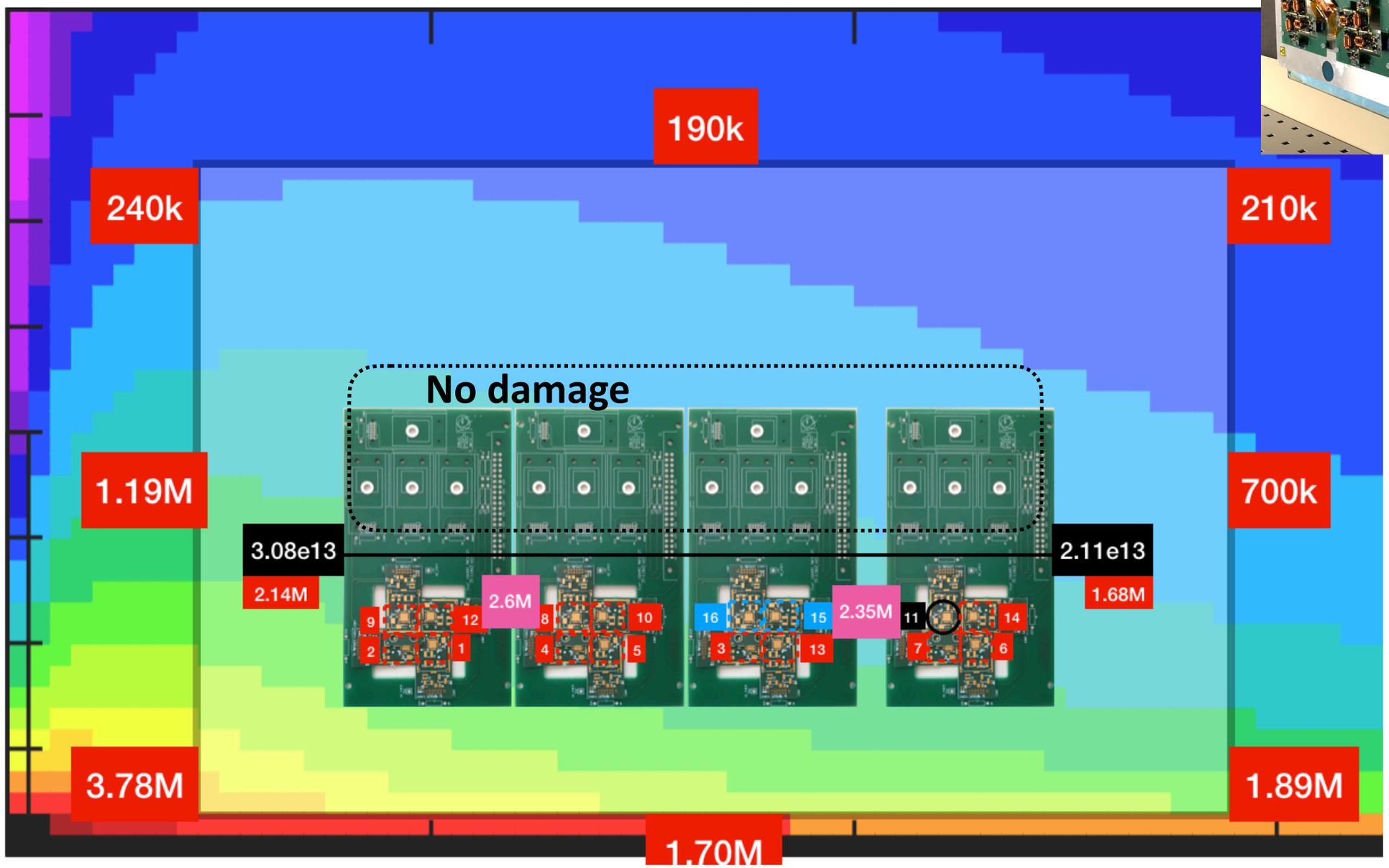


The full sequence lasts about 2 hours, with 97% of the time in “monitoring”

The results powerfully revealed some important correlation:

- **Between the damage and the integrated flux**
  - The first damage occurs after 9 days, then several samples per day
  - Only samples closer to the beam are damaged
  - Samples are damaged also after the end of the exposure
- **Between the occurrence of the damage and the disable-enable sequence**
  - Also true for the “High-Current”





Red = High-Current damage occurred during exposure
Blue = High-Current damage occurred after exposure
Black = failure

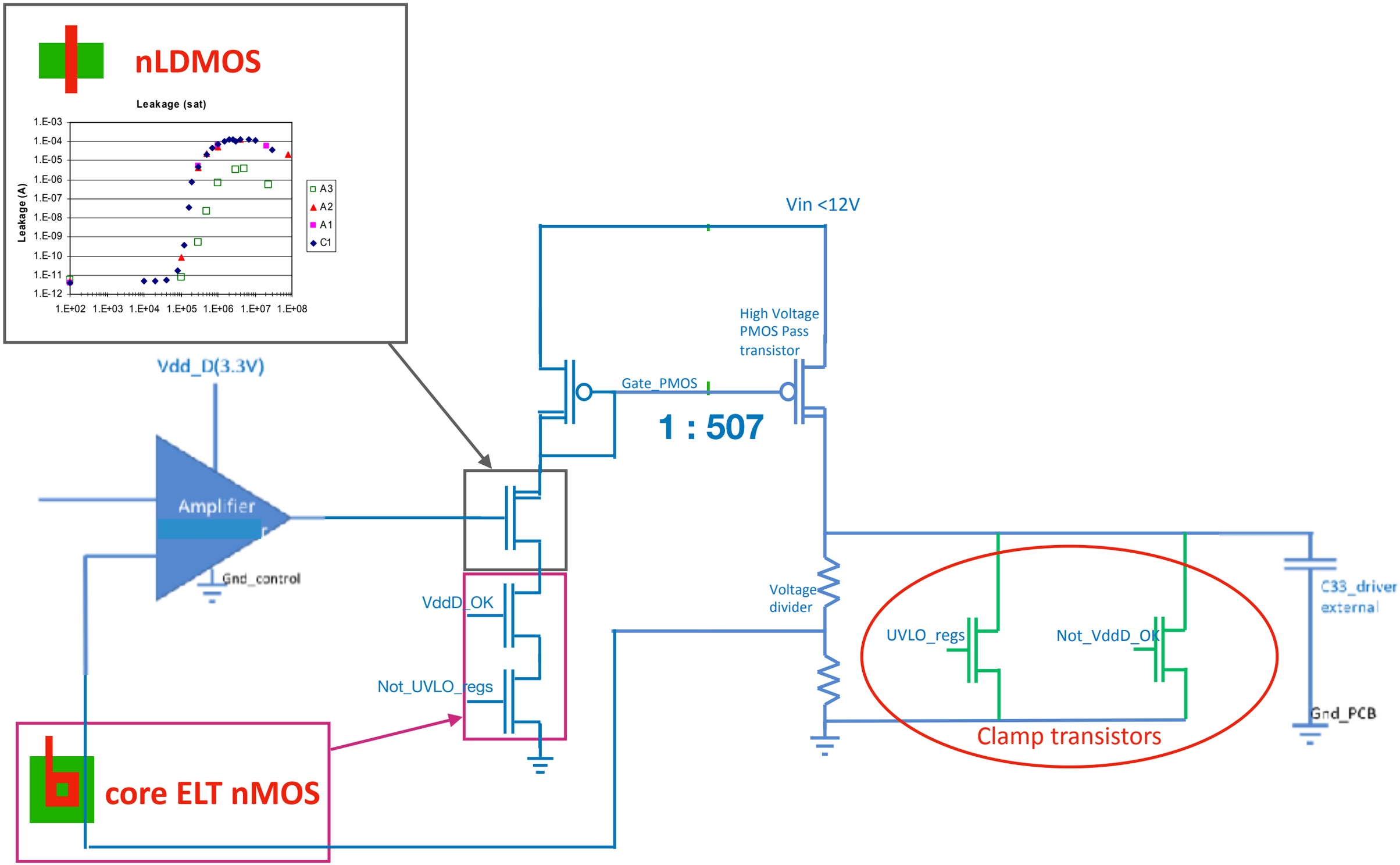
X-ray irradiation using the same enable/disable cycle as in IRRAD, and monitoring the current under UVLO thresholds, it was eventually possible to produce the same damage!

Now we had a tool to study the mechanism in detail!

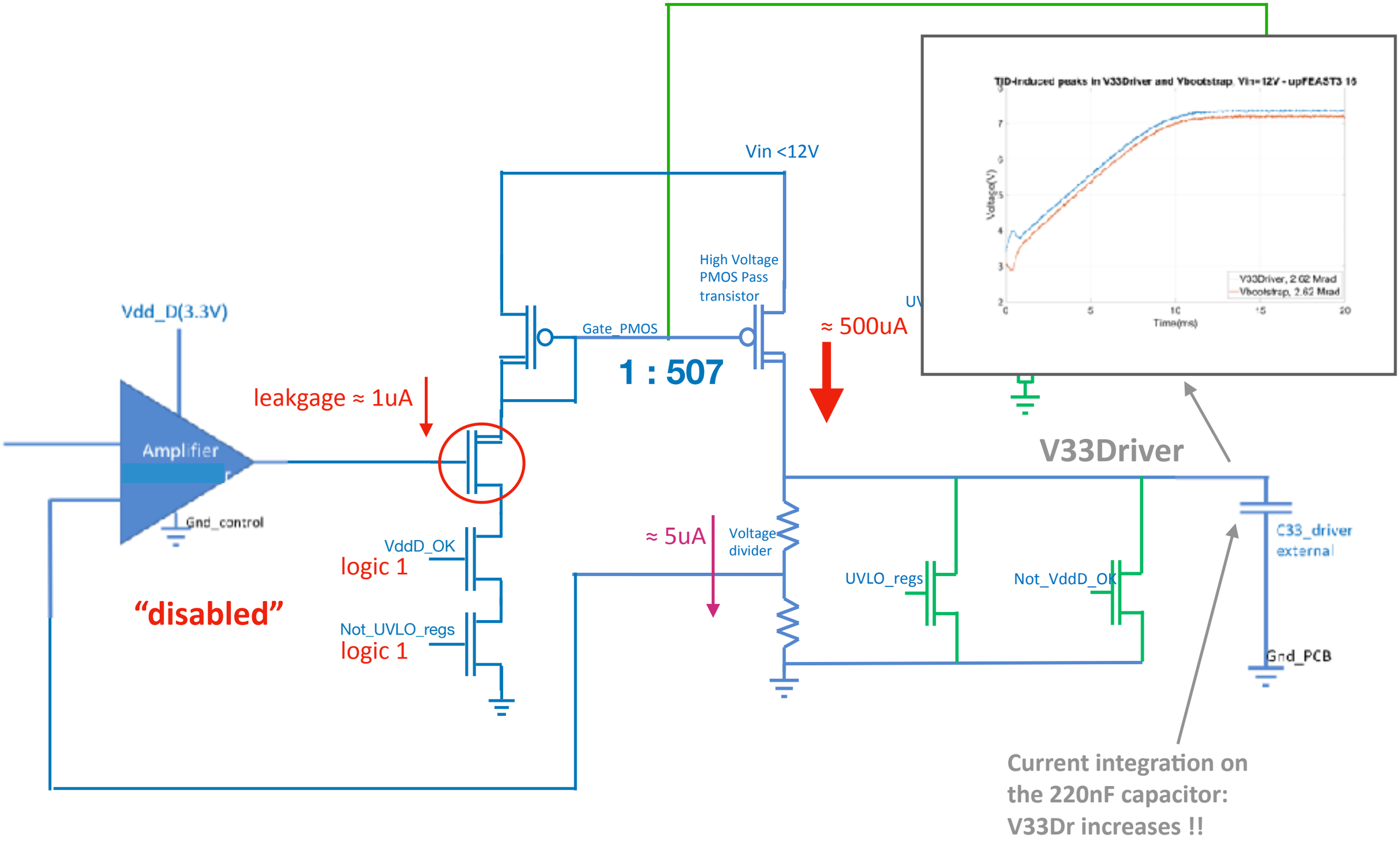
X-ray machine of the EP-ESE group

The crime reconstruction

The problem is localised in the linear regulator (V33Dr) that provides the required current to the drivers of the power transistors (HS and LS)



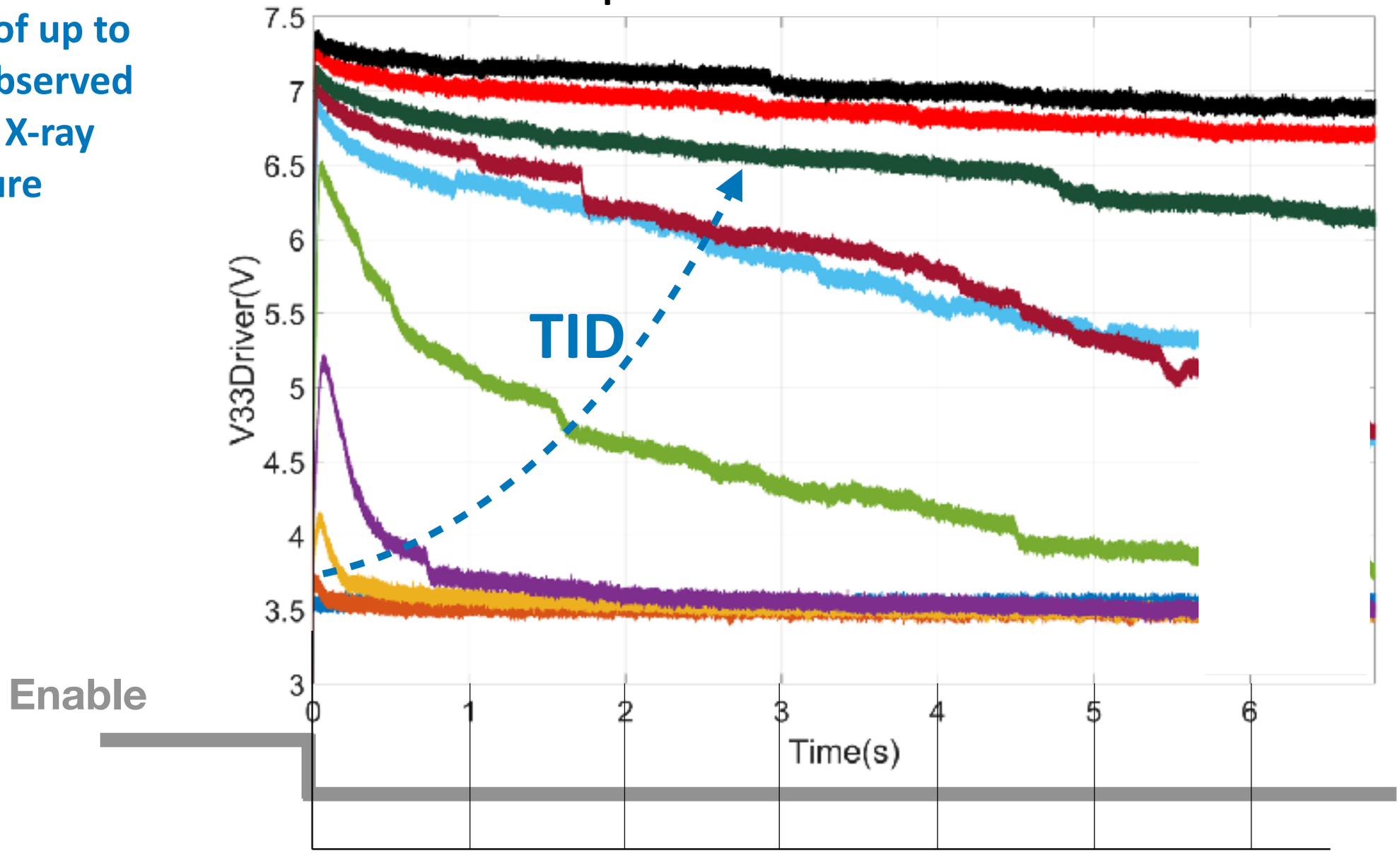
In the presence of a large TID-induced leakage in the nLDMOS, consequences appear ONLY when FEAST2 is disabled (no load for the V33Dr regulator)



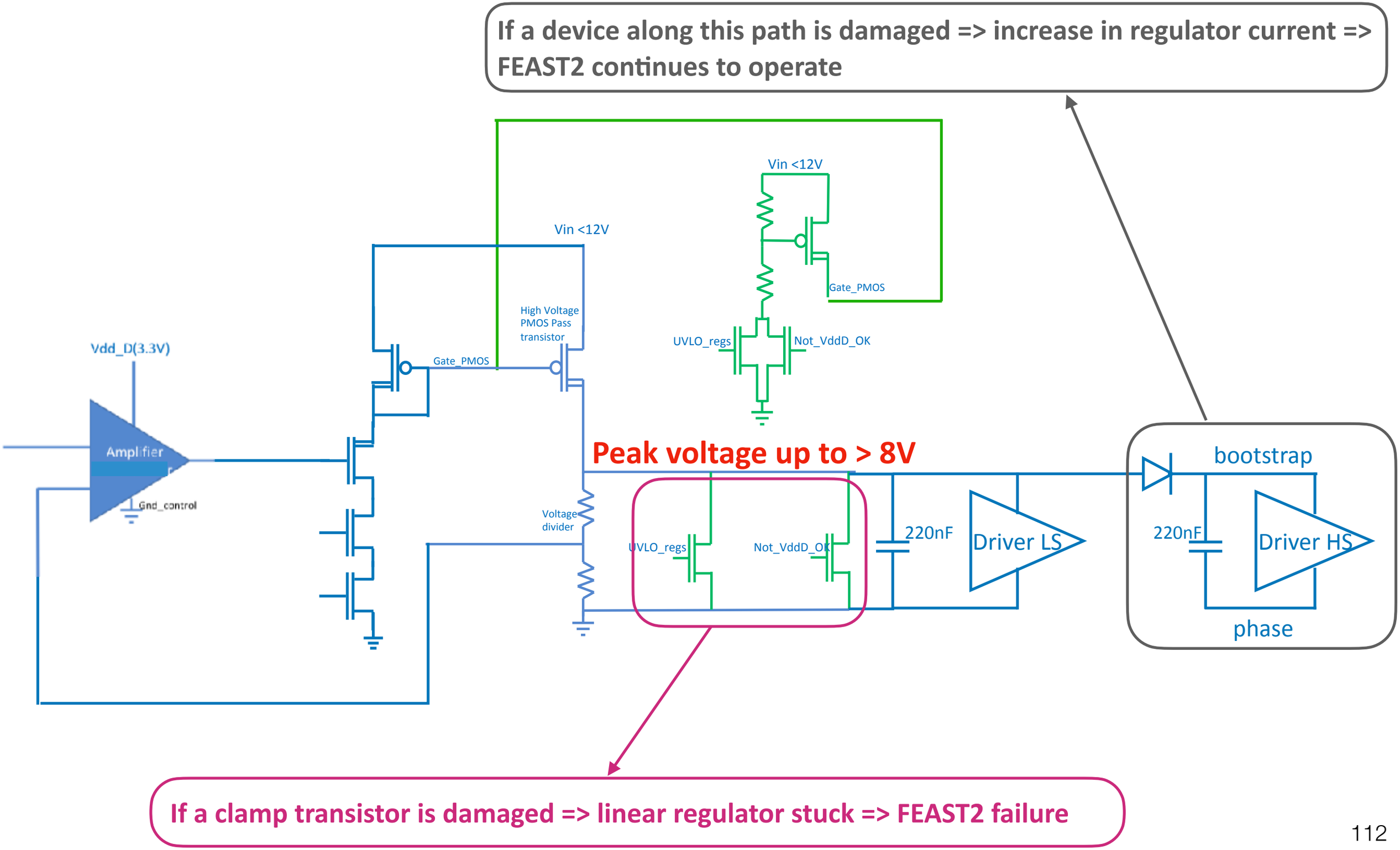
We observed a “voltage peak” on the V33Dr node when FEAST2 is disabled during X-ray exposures. The voltage peak increases with TID

Peaks of up to 8.5V observed during X-ray exposure

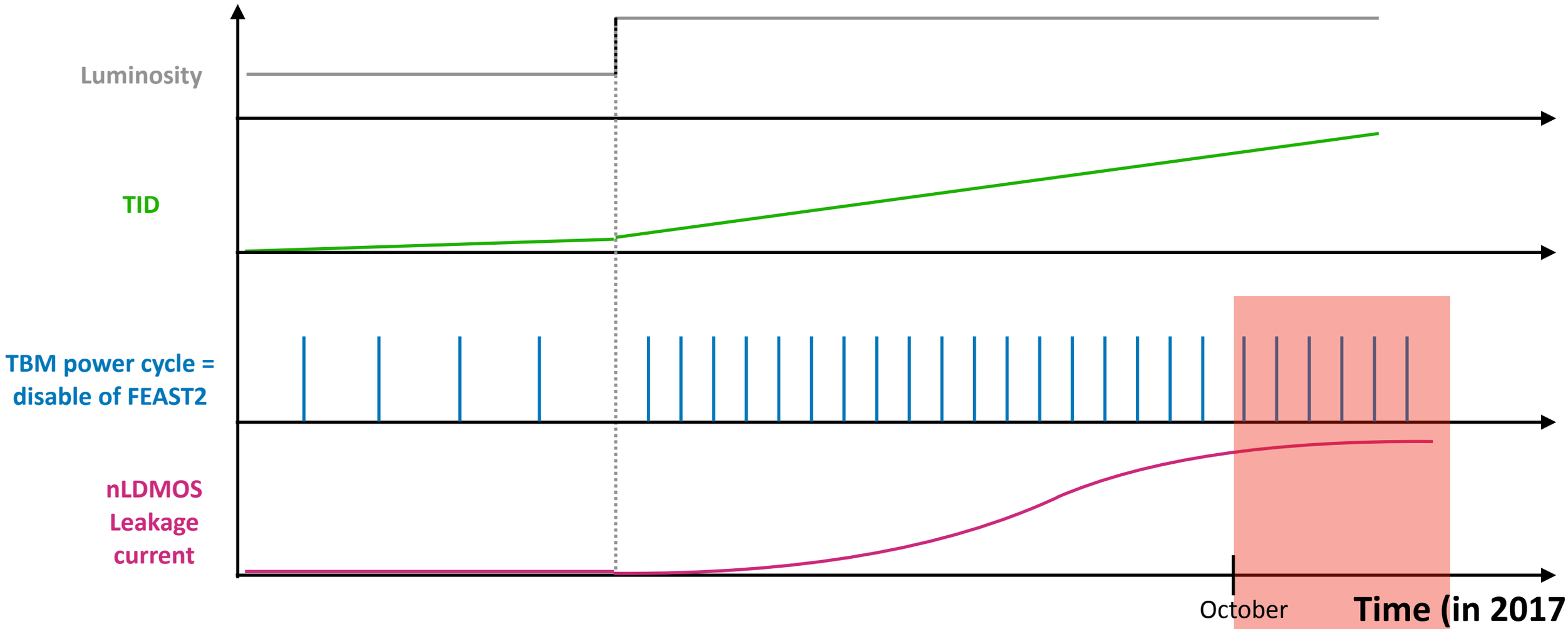
Example waveforms at the V33Dr node



The voltage at the V33Dr node goes well beyond the nominal maximum of 3.3V+10%.
This voltage stress might end up damaging a device. We have observed 2 damage mechanisms, and Failure Analysis with emission microscopy and OBIRCH have confirmed the current paths.

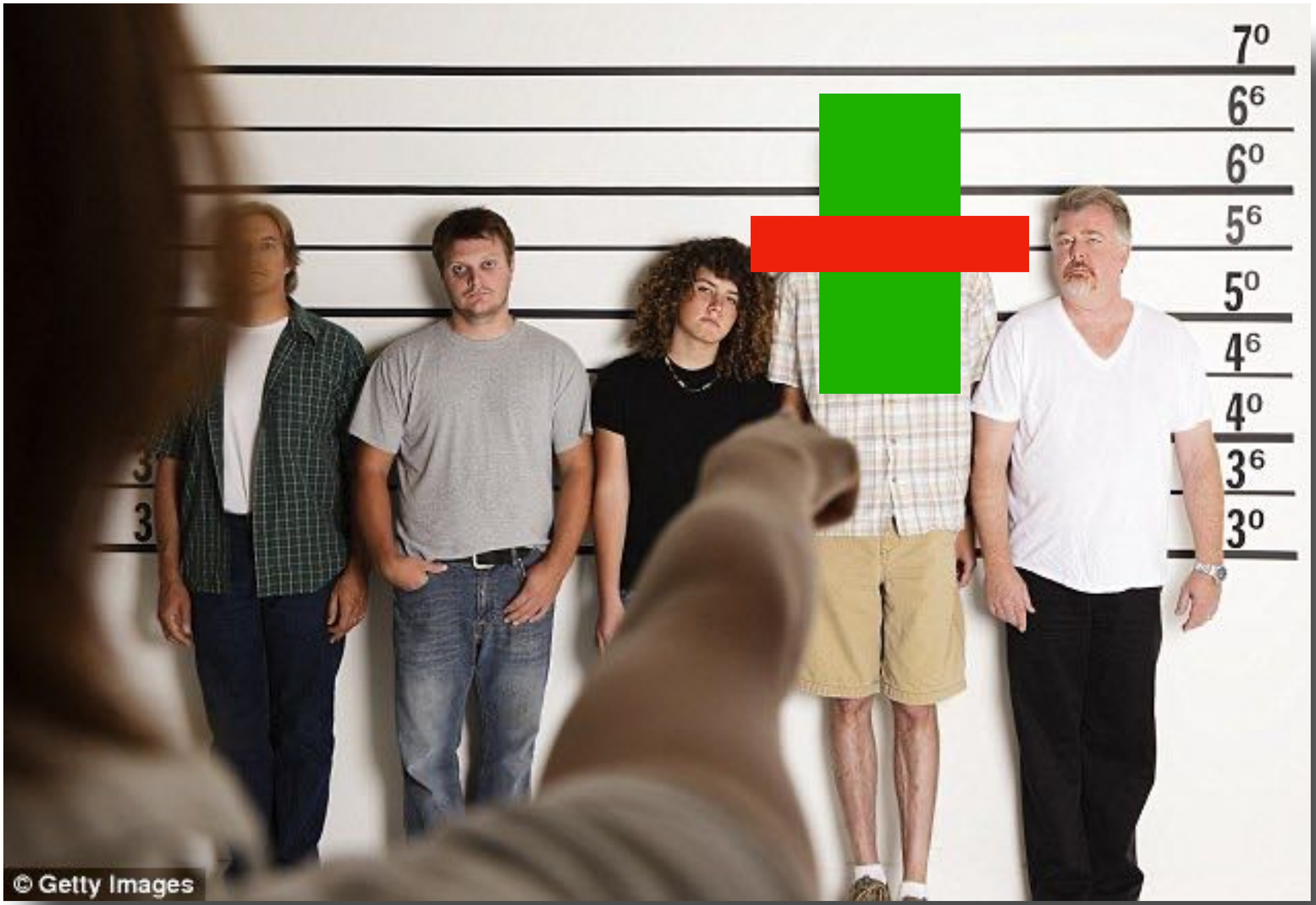


A graphical representation of the narrative



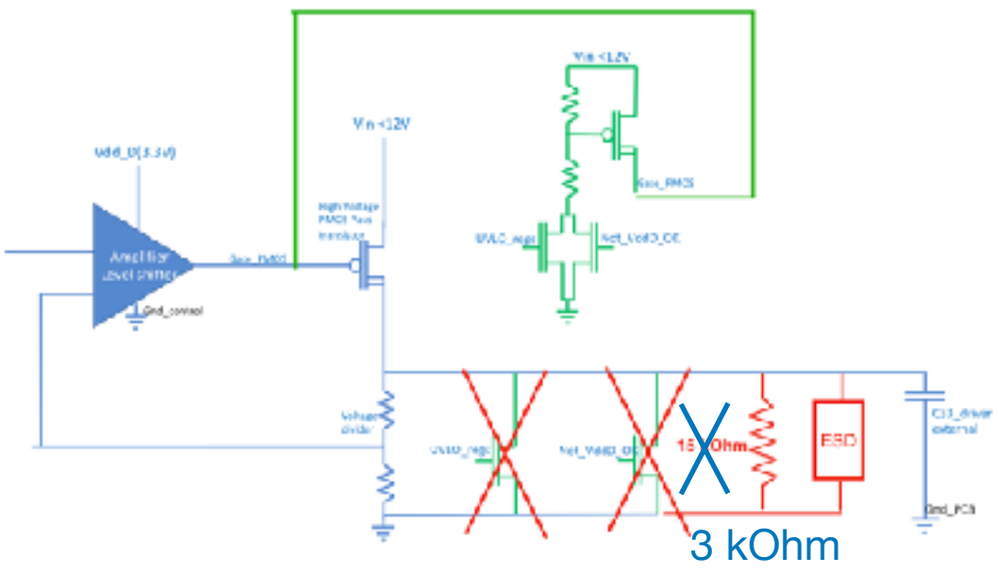
TBM requires a power cycle
=> FEAST2 is disabled while the leakage is large
=> peak voltage at V33Dr
=> damage

The perpetrator



2 easy to implement patches were used to rapidly fix the problem. Then a permanent solution was implemented in a new version of the circuit.

FEAST2.3

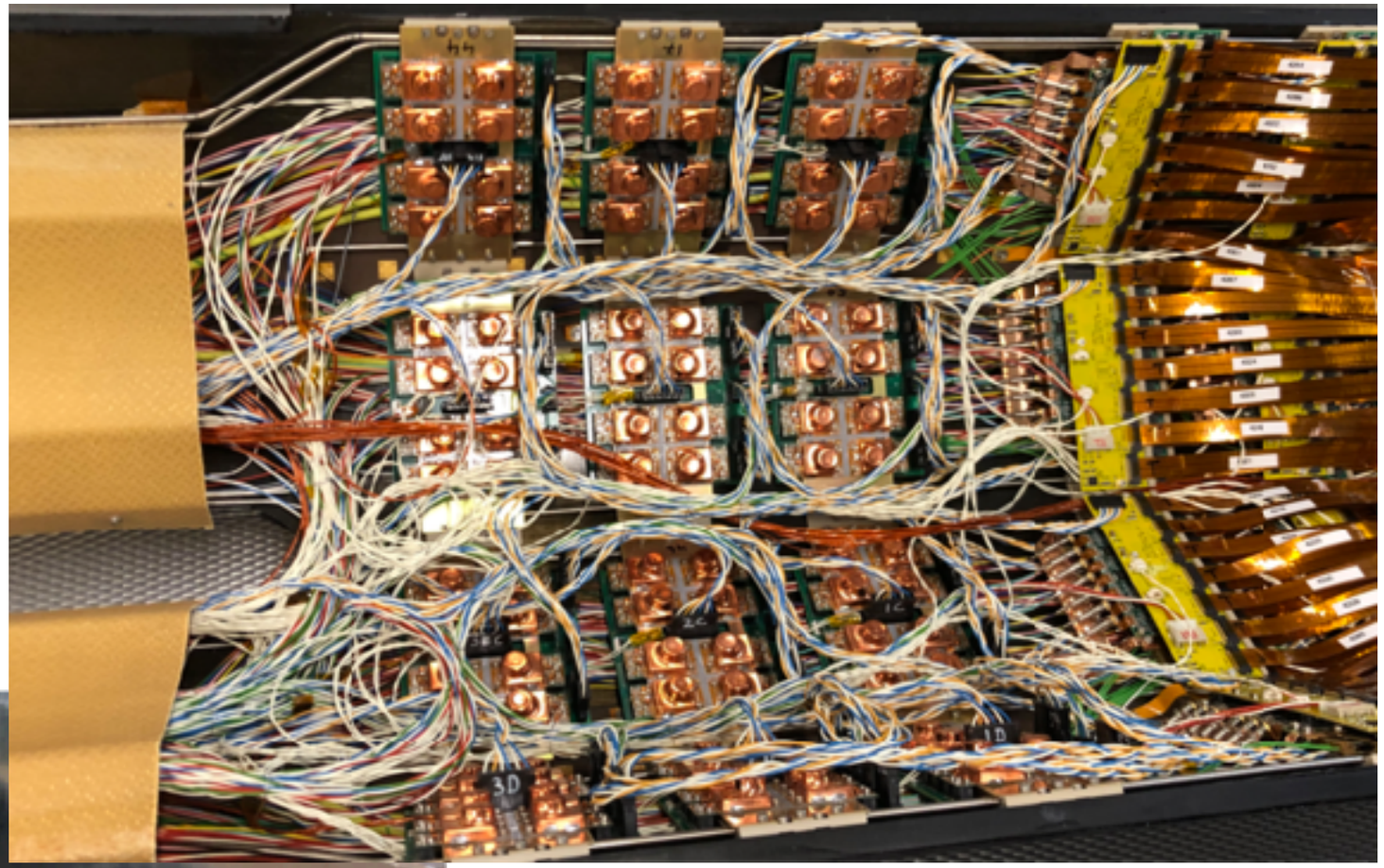


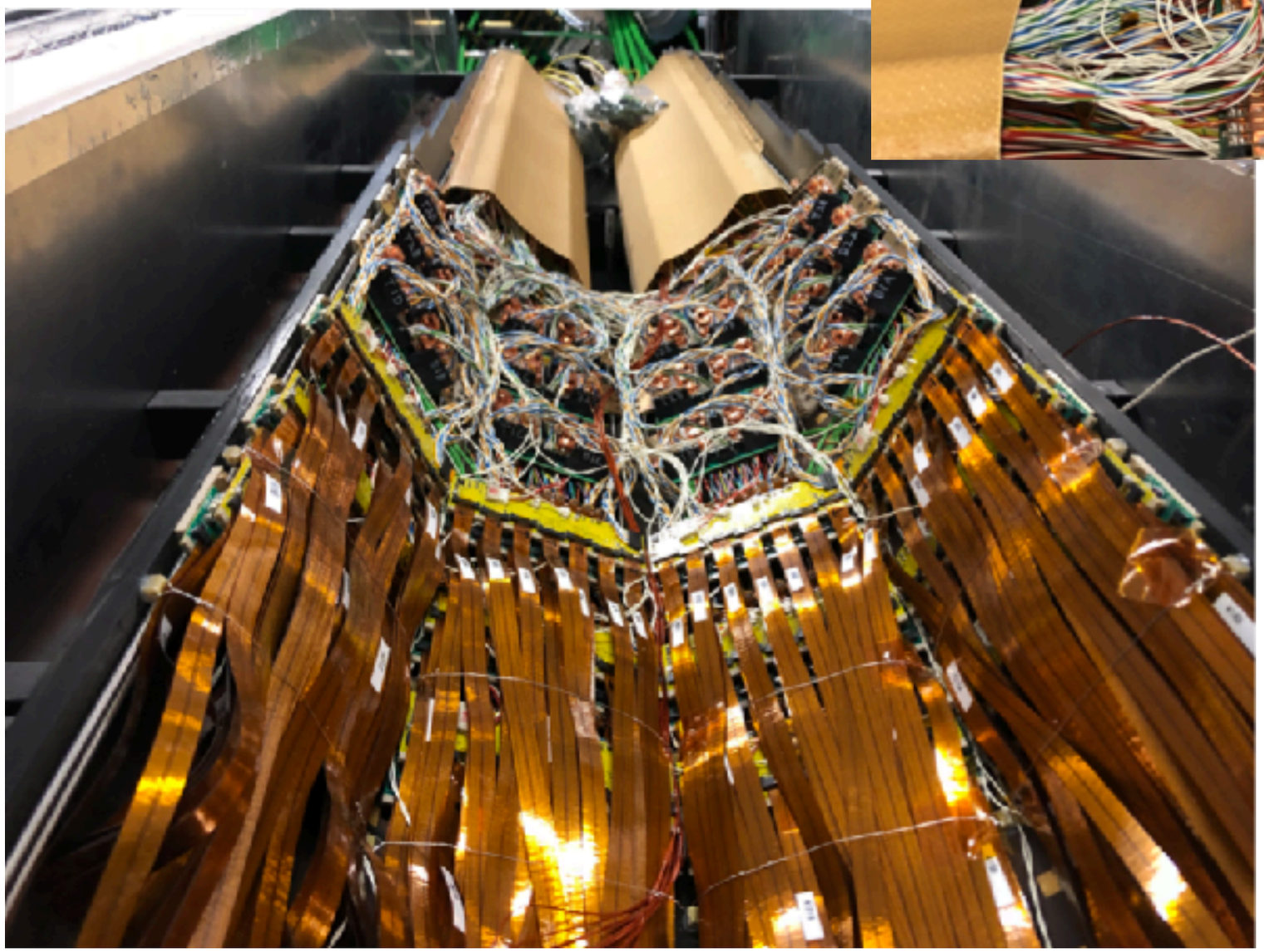
Present default version for all modules

Thoughts inspired by this FEAST2 crisis

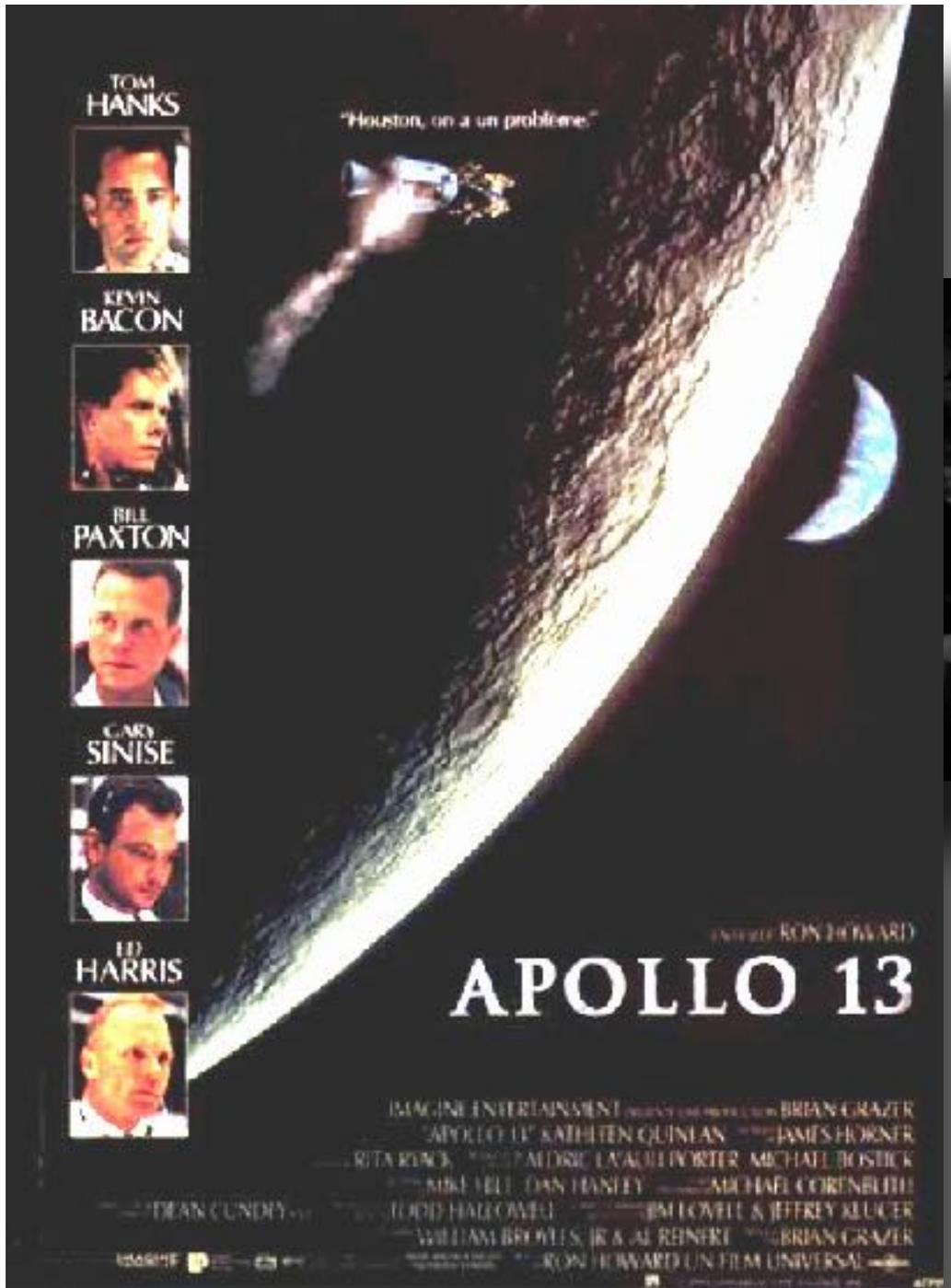
This is a very complex system

- Assembly of different sub-systems
- Unique “prototype”
- Tested in the real environment only





We are not NASA in the 1970s…



Some reasons to be grateful for our luck

- **The designers of the failing component were still around, and at CERN**
- **The problem happened to a detector that is amongst the easier to open**
- **Once understood, patches and fixes were easy to implement**
- **The problem appeared in 2017 and not in HL-LHC trackers**

**Personally I'm always ready to learn,
although I do not always like being taught**

W. Churchill