



Silicon sensors for 4D tracking

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WHY 4D TRACKING?



The search for new physics pushes forward the high-energy and high-luminosity frontiers



REQUESTS FROM THE HEP COMMUNITY



From the 2021 ECFA detector research and development roadmap, doi:10.17181/CERN.XDPL.W2EX

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REQUESTS FROM THE HEP COMMUNITY



⇒ Future HEP experiments require tracking with a timing resolution of the order of 10 ps

HOW DO WE DO 4D TRACKING?

The inclusion of track-timing in the event information has the capability of changing radically how we design experiments

Timing can be available at different levels of the event reconstruction, in increasing order of complexity:

▷ Timing in the event reconstruction → Timing Layers This is the easiest implementation, a layer ONLY for timing



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- ▷ Timing at some points along the track → 4D Tracking Tracking - Timing



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- ▷ Timing in the event reconstruction → Timing Layers This is the easiest implementation, a layer ONLY for timing
- ▷ Timing at some points along the track → 4D Tracking Tracking - Timing
- Timing at each point along the track at a high rate and high density
 - \rightarrow High Rate (HR) 4D Tracking

A very high rate represents an additional step in complication, very different read-out chip and data output organization



TIMING IN THE EVENT RECONSTRUCTION

 \rightarrow Timing allows distinguishing overlapping events by means of an extra dimension



TIMING AT EACH POINT ALONG THE TRACK

→ Massive simplification of pattern recognition, new tracking algorithms will be faster even in very dense environments



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TIMING AT THE TRIGGER LEVEL

→ Timing at the trigger decision allows reducing the trigger rate rejecting topologies that look similar



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TOWARDS 4D TRACKING

Silicon-based 4D detectors

- Low ionisation energy
- Fast signal collection
- Possibility for fine segmentation

► Signal formation

Ramo's theorem

$ightarrow \sigma_t$ ingredients

Technologies for 4D tracking

- Silicon sensors with internal gain
- ► 3D silicon sensors
- Monolithic detectors

RADIATION SIGNAL DETECTION IN Si

To directly ionize a semiconductor material, particles have to be charged

- Charged particles (e, p, π^{\pm} , K[±], μ , α particles, ions)
- Photons and neutrons have to react in the crystal to produce ionising particles, which are then detected



REVERSE BIAS & CARRIER'S DRIFT VELOCITY

Minimum bias voltage for full sensor depletion

q N d







REVERSE BIAS & CARRIER'S DRIFT VELOCITY

In a **fully depleted** sensor, the collection speed depends on the carrier transit time in the depleted region (d)



v_{drift}: carrier's drift velocity
 v_{sat}: saturated drift velocity
 μ: carrier's mobility



[Sze, Semiconductor devices, Wiley&Sons, 2012]

SIGNAL FORMATION – INDUCED CURRENT

The charge carrier's motion induces a variable charge on the read-out electrode

The signal ends when all the charges are collected



Signal shape is determined by Ramo's theorem:



A TIME-TAGGING DETECTOR



Time is set when the signal crosses the comparator threshold

The timing capabilities are determined by the characteristics of the signal at the output of the pre-amplifier and by the TDC binning

Strong interplay between sensor and electronics

A TIME-TAGGING DETECTOR



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FAST TIMING - THE INGREDIENTS

The time resolution σ_t of a detector can be expressed as the sum of different contributors

$$\sigma_t^2 = \sigma_{Jitter}^2 + \left(\sigma_{Landau} + \sigma_{Total} \right)^2 + \sigma_{Distortion}^2 + \sigma_{TDC}^2$$

\rightarrow In order to achieve a timing resolution of ~ 10 ps, each of the terms contributing to σ_t needs to be minimised independently

THE JITTER

The jitter term is due to the effect of the noise, N, when the signal is approaching the threshold, V_{th} , with a slope dV/dt

$$\sigma_{\text{Jitter}} = \frac{N}{dV/dt} = \frac{t_{\text{rise}}}{S/N}$$

 σ_{Jitter} can be minimised by shortening the signal rise time, t_{rise} , and by increasing the signal to noise ratio, S/N

 \rightarrow N is dominated by the electronic noise



SIGNAL DISTORTION



The key to good timing is the uniformity of signals

From Ramo's theorem, drift velocity and weighting field need to be as uniform as possible



- saturated drift velocity
- ▷ strip implant ~ strip pitch >> thickness → parallel plate geometry

The energy deposited by a particle crossing the sensor follows a Landau distribution Signals with different amplitudes cross a fixed threshold at different times – **time walk effect**

 σ_{Total} < 10 ps \rightarrow can be minimised by an appropriate electronic circuit Ionization



→ On paper both circuits seem feasible, in practice **ToT is much easier to implement**

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IRREDUCIBLE LANDAU NOISE

The signal shape varies on a event-by-event basis due to the random nature of electron-hole pairs creation along the particle path while traversing the sensor thickness



Simulations done using Weightfield2 [l.infn.it/wf2]

 \rightarrow It depends on the sensor thickness and is absent in the 3D sensor technology

HIGH LANDAU TAILS

4.5e-05 4.5e-05 4e-05 3e-05 2.5e-05 2.5e-05 2.5e-05 2.5e-05 1.5e-05 1.5e-05

$\sigma_{Landau} \times \sigma_{Ionisation}$

Due to the correlation between large signals and non-uniform ionisation

The events in the high tail of the Landau distribution of charge are mostly due to the presence of localised clusters of ionisation

The high non-uniformity of the ionisation worsens the time resolution of such events



HPK 4x4 pre-Rad @210V - Time Resolutions for different amplitude ranges

TDC BINNING

 $\sigma_{TDC} = \frac{25 \text{ps}}{\sqrt{12}} \sim 7 \text{ ps}$ considering 25 ps binning of the High Precision TDC from CERN

 \rightarrow Precise time-to-digital conversion requires power



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ONE SENSOR DOES NOT FIT ALL

The goal of a sensor designer is to minimise the differences in the sensor's output, providing well defined, uniform current signals to the electronics

Silicon sensors for tracking come in many shapes, fitting very different needs:

- \triangleright Spatial resolution: from a few μ m to mm (pixels, strips)
- ► **Area**: from mm² up to hundred of square meter
- ▷ **Radiation damage**: from nothing to > 1E16 n_{eq}/cm^2 (3D, thin planar, thick planar)

Likewise, Silicon sensors for time-tracking are being developed to fit different needs with respect to the requested time and space resolutions

The geometries above are combined with:

- ▷ Excellent time precision ~ 10-20 ps per plane
- ▷ Very good precision ~ 30-50 ps per plane
- ▷ Good time precision ~ 50-100 ps per plane

Simulation

ASIC designers need to test their solutions on a realistic set of current signals that reproduce the full variability of the sensor's output

\rightarrow Good sensor simulation is necessary to achieve excellent time resolution

In the past few years, several silicon simulators programs have come to the market and now are freely available:

- ▷ Weightfield2, <u>l.infn.it/wf2</u>
- ▷ KDetSim, <u>kdetsim.org/</u>
- ▶ TRACS (TRAnsient Current Simulator), github.com/IFCA-HEP/TRACS & doi:10.1016/j.nima.2018.11.132
- ► TCoDE, doi:10.1088/1748-0221/16/02/p02011 & doi:10.3389/fphy.2022.804752

ELECTRONICS - THE PRE-AMP CHOICHE



INTERPLAY OF POWER, PIXEL SIZE & ELECTRONICS

The pixel size, the spatial and temporal resolutions are strongly interconnected \rightarrow each application will need a specific optimisation

	Temporal resolution	Spatial resolution
Pixel size	Relevant	Very relevant
Area needed by electronics	Larger	Smaller
Power consumption	Very high	Rather low

Power will determine the architecture of 4D tracking detectors

Power density limits the pixel size and the achievable temporal resolution



SENSORS + ELECTRONICS

Let's consider a pixel size ~ $100 \times 100 \ \mu m^2$

- > Can we produce a sensor with small pixel and high fill factor?
- Can we fit the electronics?
 - \rightarrow the preamplifier does not scale with the technological node
 - \rightarrow memory and TDC do

Example: TDC evolution



⇒ High rate 4D Tracking requires either 65 nm or 28 nm electronics

Planar Silicon Sensors with Internal Gain

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SENSORS WITHOUT INTERNAL GAIN

The most advanced 4D-tracker detector using planar sensors in a hybrid configuration is the NA62 GigaTracker



Sensos thickness = 200 μ m Sensor size = 60.8 \times 27 mm² Pixel size = 300 \times 300 μ m²

The TDCpix ASIC of the A62 GigaTracker ▷ Designed in CMOS 130 nm technology ▷ 40 × 45 pixels

 \rightarrow Single hit temporal resolution of about 130 ps

⇒ The only 4D tracking system on a working experiment

SIGNAL OF ONE e/h PAIR

(Simplified model for pad detectors)

Considering one single electron-hole pair:

- ▷ The integral of the current is equal to the electric charge, q
- However, the shape of the signal depends on the thickness d
 thinner detectors have higher slew rate, dV/dt



 $\int [i_{el}(t) + i_{h}(t)] dt = q$

One e/h pair generates higher current in thin detectors $\frac{1}{d}$

1/d: weighting field of a parallel plate capacitor

INITIAL CURRENT & THICKNESS

(Simplified model for pad detectors)

Thick detectors have higher number of charges: $Q_{tot} \sim 75~q~d$ (assuming a MIP generates 75 e/h per μm)

However, each charge contributes to the initial current as:

$$i \propto q v_{drift} \frac{1}{d}$$

The initial current for a silicon detector does not depend on how thick (d) the sensor is:

$$i = Q_{tot} v_{drift} \frac{1}{d} = (75 \text{ q/d}) v_{drift} \frac{1}{d} \sim 75 \text{ q} v_{drift} \sim 1-2 \mu \text{A}$$

 \rightarrow Initial current = constant



SIGNAL & THICKNESS



Thick detectors have longer signals, not higher signals

 \Rightarrow We need internal gain to boost the signals

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INTERNAL GAIN IN SILICON DETECTORS

Gain in silicon detectors is commonly achieved in several types of sensors It's based on the avalanche mechanism that starts in high electric fields: V ~ 30 V/ μ m

Gain:
$$G = e^{\alpha l}$$
 $\alpha_{e,h}(E) = \alpha_{e,h}(\infty) * \exp\left(-\frac{b_{e,h}}{|E|}\right)$

I: path length inside $\alpha =$ the high field region $\alpha \sim$

 α = strong E dependence $\alpha \sim 0.7$ pair/µm for electrons $\alpha \sim 0.1$ for holes

Concurrent multiplication of electrons and holes generate very high gain

Silicon devices with gain: SiPM: gain ~ 10^4 APD: gain ~ 50 - 500LGAD: gain ~ 10 - 30



LOW-GAIN AVALANCHE DIODES



Must have:

- ➤ Large dV/dt
- > Segmentation
- Radiation hard

The game changer is the introduction by CNM of the LGAD^[*] idea:

- > Add a thin layer of doping to produce low controlled multiplication
- > This idea retains almost (segmentation) the benefit of standard silicon sensors
- \rightarrow UFSD^[**]: LGAD sensors, optimised for timing
- [*] LGAD = Low-Gain Avalanche Diodes
- [**] UFSD = Ultra-Fast Silicon Detectors
GAIN & SIGNAL SHAPE



GAIN & SENSOR THICKNESS

The rate of particles produced by the gain G does not depend on the thickness, d (assuming saturated drift velocity, v_{sat})



$$dN_{gain} \propto 75 (v_{sat} dt) G$$

 \rightarrow Constant rate of production

However, the initial value of the gain current depends on the thickness (via the weighing field)

di
$$\propto dN_{gain} q v_{sat} \frac{1}{d}$$

GAIN & SIGNAL STEEPNESS



GAIN & SIGNAL STEEPNESS



LANDAU NOISE FROM LGAD SENSORS



⇒ Thin sensors minimise the irreducible contribution of the non-uniform ionisation to the timing resolution

JITTER FROM THE ELECTRONICS



⇒ A low-noise electronics allows to reach optimal time resolution at low gain

JITTER FROM THE SENSOR – SHOT NOISE



MEASURED TIME RESOLUTION



50 μ m LGAD sensor \rightarrow **30 ps time resolution**

Value of gain ~ 20

TIME RESOLUTION WITH THICKNESS



Comparison WF2 Simulation - Data Band bars show variation with temperature (T = -20C - 20C), and gain (G = 20 -30)

UFSD temporal resolution improves in thinner sensors:

 \rightarrow reasonable to expect 10 – 20 ps for 10 – 20 μm thick sensors

⇒ Be aware: very difficult to do timing with small signals, due to power consumption increases

LGAD – THE STATE-OF-THE-ART



LGAD – THE STATE-OF-THE-ART



The ATLAS and CMS timing layers will use about 25 m² of UFSD sensors

- ▷ Very well tested
- ightarrow Will be used up to ~ 2E15 n_{eq}/cm²
- \triangleright Gain ~ up to 40 when new \rightarrow up to 20 fC
- ▷ Signal duration ~ 1 ns
- \triangleright Low noise
- ▷ Rate ~ 50-100 MHz
- Excellent production uniformity

Shortcomings:

- \succ Large no-gain area between pads \rightarrow not suitable for 4D tracking
- ▷ Intrinsic temporal resolution ~ 25 30 ps due to Landau noise
- ▷ Poor spatial resolution \rightarrow 1.3 mm/V12 ~ 375 µm

TRENCH ISOLATED LGAD – ENABLING 4D



To minimise the no-gain region, the interpad isolating structures are substituted with trenches filled with oxide

No-gain width: 50 – 80 μ m \rightarrow 0 – 10 μ m

This solution enables the design of small pixels, hence precise position reconstruction



AC-LGAD & RESISTIVE READ-OUT



A breakthrough design toward 4D tracking \rightarrow LGAD with resistive read-out

Resistive Silicon Detectors – RSD

1. The signal is formed on the n+ electrode

2. The AC pads offer the smallest impedance to ground for the fast signal

3. The signal discharges to ground

In resistive readout, the signal is naturally shared among pads (4-6) without the need of B field or floating pads Thanks to the internal gain, full efficient even with sharing

AC-LGAD – EXAMPLE OF SIGNAL SHARING



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RSDs reach a spatial resolution that is about 5% of the distance between pads

 \rightarrow ~ 5 μm resolution with 150 μm pitch

RSDs have the temporal resolution typical of LGAD sensors ~ 30 – 40 ps

ADVANTAGES OF A RESISTIVE READ-OUT



- ▷ It reduces the number of pixels by a large factor (~ 50)
- hightarrow An RSD sensor with a 200 μ m pitch has the same spatial precision of a traditional sensor with 25 μ m pitch
- ▷ The pixel size is determined by occupancy
- ▷ Large area for the electronics, much more power per pixel available
- ▷ Low material budget

LGAD RADIATION HARDNESS

The radiation deactivates the acceptor atoms in the gain layer region, reducing the signal multiplication power of the LGAD sensors

$$\mathbf{p}^+(\Phi) = \mathbf{p}^+(\mathbf{0}) \ \mathbf{e}^{-\mathbf{c}\Phi}$$



Concluded R&D

- ▷ Defect engineering of the gain implant
- ▷ Carbon co-implantation mitigates the gain loss after irradiation
- ▷ Modification of the gain implant profile
- Narrower Boron doping profiles with high concentration peak are less prone to be inactivated
 - \rightarrow Unchanged performances up to 2E15 n_{eq}/cm^2

Present R&D towards 1E17 n_{eq}/cm²

- ▷ Compensation: gain implant obtain as difference of p- and n- doping
 - \rightarrow Concurrent acceptor and donor removal might limit the disappearance of effective doping
- ▷ Carbon shield:
 - \rightarrow A deep implant of carbon might prevent defects to reach the gain implant

3D Silicon Sensors

3D SENSORS – MOTIVATION

Original idea: S. Parker et al., <u>doi:10.1016/S0168-9002(97)00694-3</u> (1997)

Key points:

- \triangleright Short inter-electrode drift distance (tens of μ m) give rise to extremely fast signals (d<<L)
- ▷ Active volume and electrode shape can be designed for maximum performance
- ▷ Unmatched radiation hardness (> 1E17 n_{eq}/cm², M. Manna et al., <u>doi:10.1016/j.nima.2020.164458</u>)
- ▷ 3D columnar geometry is a production-ready technology (ATLAS IBL, CMS PPS)



Charge deposition distance is decoupled from electrode distance

3D SENSORS – OPTIMISED GEOMETRY

Remember: non-uniformities in the weighting field and charge carrier velocities inside the detector sensitive volume give the ultimate limit on the time resolution that can be achieved with a 3D sensor



3D sensor layout is a key for its performance

 \rightarrow TimeSPOT 3D trench-type silicon pixel detectors

THE TRENCH-TYPE 3D PIXEL



- 55 μm x 55 μm pixels (to be compatible with existing FEE, for example the Timepix family ASICs)
- ▷ In each pixel a 40 µm long n+ trench is placed between continuous p+ trenches used for the bias
- ▷ 150 µm-thick active thickness, on a 350 µm-thick support wafer
- hinspace The collection electrode is 135 μm deep



3D SENSORS – SIGNALS



The inefficiency (at normal incidence) due to the 3D pixel dead-area of the trenches can be recovered by tilting the sensors around the trench axis at angles larger than 10°

\Rightarrow The intrinsic timing resolution of the trench-type 3D sensors is ~ 10 ps

FRONT-END ELECTRONICS FOR 3D SENSORS

TIMESPOT 1



Reduced size (32x32 = 1024 pixels, total area 6 mm²) Complete set of functionalities for pixel readout with timing Max sustainable rate 3 MHz/pixel (1 TDC per pixel) 1.8 x 1.8 mm² sensitive area 50 μm pixel pitch (in y direction)

Results on timing performace

- TDC: σ_{TDC} ≈ 20 ps, in average simulated < 10 ps
 Worsened timing performance and dispersion due to the master clock jitter inside the pixel matrix
- ▷ AFE: $\sigma_{AFE} \approx 40$ ps, in average This value is limited by the performance of the TDC
- ▷ The next version of the ASIC is in preparation

Monolithic Design

THE MONOLITHIC TECHNOLOGY



MONOLITHIC WITHOUT INTERNAL GAIN

CMOS technology

FASTPIX is a 180 nm CMOS monolith project aiming at combining temporal stamping with excellent position precision

Lateral doping gradient leads to accelerated charge collection Resolution of ~ 120 ps

Very small pixels

MiniCACTUS is a 150 nm CMOS monolith project

Front-end mostly optimized for 1 mm^2 pixels with peaking time of 1 - 2 ns @ 1 - 2pFResolution of ~ 90 ps

Large pixels: 0.5 x 1 mm²

Seed-pixel time residuals after time-walk correction





MONOLITHIC WITHOUT INTERNAL GAIN

SiGe BiCMOS technology

MonPicoAD project

Exploit SiGe performances (extremely low noise) Exagonal pads: 65 μm About 25 μm depletion Thinned to 60 μm Resolution of ~ 36 ps Very small pixels



MONOLITHIC WITH INTERNAL GAIN

SiGe BiCMOS technology

This is a very powerful research path pursued by the *Monolith* project

Monolith merges low noise from SiGe with high dV/dt from multiplications It aims at reducing the Landau term by using very thin sensors, and high pixelation by buring the high-field

away form the surface junction

Sensor thickness: 5 μ m

Resolution of ~ 25 ps (very preliminary)



Placement of gain layer deep inside sensor:

De-correlation from pixel implant size/geometry —> high pixel granularity possible (*spatial precision*) Only small fraction of charge gets amplified —> reduced Landau charge fluctuations (*timing precision*)

Power & More

POWER NEEDS

	Name	Sensor	Node [nm]	Pixel size	σ _t [ps]	Power [W/cm²]
Hybrid	ETROC	LGAD	65	$1.3 \text{ x} 1.3 \ \mu\text{m}^2$	~ 40	0.3
	ALTIROC	LGAD	130	$1.3 \ x \ 1.3 \ \mu m^2$	~ 40	0.4
	TDCpix	PiN	130	$300 \text{ x} 300 \ \mu m^2$	~ 120	0.45 + 0.2
	TIMEPIX4	PiN, 3D	65	55 x 55 μm²	~ 200	0.8
	TimeSpot1	3D	28	55 x 55 μm²	~ 30 ps	5 – 10
Monolithic	FASTPIX	monolithic	180	20 x 20 μm²	~ 130	40
	miniCACTUS	monolithic	150	0.5 x 1 mm ²	~ 90	0.15 – 0.3
	MonPicoAD	monolithic	130 SiGe	25 x 25 μm²	~ 36	40
	Monolith	LGAD monolithic	130 SiGe	25 x 25 μm²	~ 25	40

The present ATLAS, CMS, and LHCb silicon trackers generate about $0.5 - 1 \text{ W/cm}^2$ A 3kW wall electric heater has a power dissipation of < 1W/cm²

READ-OUT & ALGORITHMS



If we succeed in having the sensors and the read-out chip, still lot of work needed

Taking advantage of high rate 4D Tracking requires a very complex back end:

- > Very fast data transfer
- Real time tracking requires the development of specific 4D tracking → sometimes called *retina*, being pursued by several groups

SUMMARY

A new generation of detectors able to measure both time and space with high accuracy are being developed

- ▷ LGAD are the proposed technology for ATLAS and CMS High-Luminosity upgrades
- ▷ R&D on different technologies to develop a full 4D tracking system
- It is a challenging and beautiful development that requires a collective effort to succeed
- > There is no 'one technology fits all'
 - depending on segmentation, precision, radiation levels and other factors the best solution changes

⇒ The path toward new detectors for the forthcoming 4D tracking at future HEP experiments is traced

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- ⊳ RD50, CERN

BACKUP

GAIN MEASUREMENT



GAIN = (Signal area LGAD)/(Signal area PiN)



TCT Setup from Particulars Pico-second IR laser at 1064 nm Laser spot diameter ~ 50 μm Cividec Broadband Amplifier (40dB) Oscilloscope Lecroy 640Zi Room temperature


JITTER & LANDAU NOISE IN LGADS

If you consider only Jitter, the best choice is to trigger above ~ 5-10% since at the beginning the slope is not at maximum



The best level is determined by the electronics turn-on:

- ▷ Very fast electronics (SiGe?)
- ▷ Very small load capacitance

Towards a Radiation Resistant Design



The acceptor removal mechanism deactivates the p⁺-doping of the **gain layer** with irradiation according to

 $p^{+}(\Phi) = p^{+}(0) \cdot e^{-c_{A}\Phi}$

where c_A is the acceptor removal coefficient c_A depends on the initial acceptor density, $p^+(0)$, and on the defect engineering of the gain layer atoms



A new Paradigm – Compensation

Impossible to reach the design target with the present design of the gain layer

Use the interplay between acceptor and donor removal to keep a constant gain layer active doping density

Many unknown:

- ▷ donor removal coefficient, from $n^+(\Phi) = n^+(0) \cdot e^{-c_D \Phi}$
- interplay between donor and acceptor removal (c_D vs c_A)
- effects of substrate impurities on the removal coefficients



LGAD IN CT-PPS

The CMS TOTEM Precision Proton Spectrometer (CT-PPS) aims at measuring the surviving scattered protons on both sides of CMS in standard LHC running conditions \rightarrow 1 plane of LGAD has been installed on both sides of CT-PPS in 2017

 $\sigma_{\Delta t} = 10 \text{ps}$ \approx

 $2 \mathrm{\,mm}$



> Aim: disentangle primary vertex from pile-up



First LGAD installation in High Energy Physics